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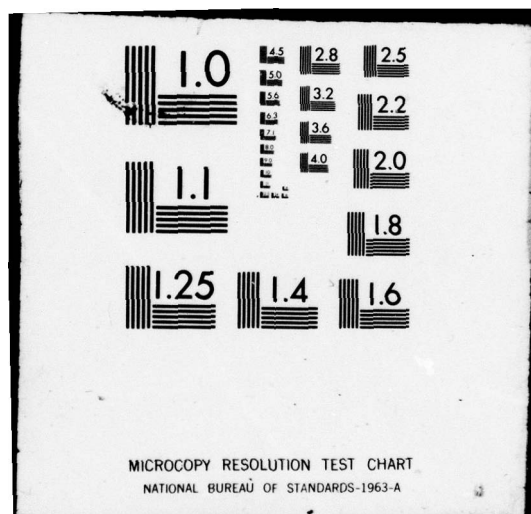
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An AC Large Signal Model for the GaAs MESFET

A. Madjar
F. J. Rosenbaum
Department of Electrical Engineering
Washington University
St. Louis, MO 63130

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August 1979

Final Report for Period 1 January 1978 - 31 July 1979

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Prepared for:

Naval Research Laboratory
4555 Overlook Avenue, S.W.
Washington, D.C. 20375

79 07 23 184

9. PERFORMING ORGANIZATION NAME AND ADDRESS Washington University Department of Electrical Engineering St. Louis, MO 63130	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61153N-21 RR021-03-046 R08-64.101
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory 4555 Overlook Avenue, S.W. Washington, D.C. 20375	12. REPORT DATE August 1979 13. NUMBER OF PAGES 213
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report) UNCLASSIFIED 16. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Approved for Public Release - Distribution Unlimited	
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	

6 AN AC LARGE SIGNAL MODEL
FOR THE GaAs MESFET.

9 Final rept. 1 Jan 78 - 31 Jul 79.

10 Asher Madjar and Fred J. Rosenbaum
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11 AUGUST 1979

12 217p.

15 N00014-78-C-0256

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17 RR02103p46

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LIST OF SYMBOLS

a	Epitaxial layer thickness
D	Diffusion coefficient
D_L	Low field diffusion coefficient
D_H	High field diffusion coefficient
d	Transition region height
$d_l(x)$	Neutral channel height
E	Electric field
E_c	Critical electric field for velocity saturation
g_m	Transconductance
g_d	Drain conductance
I_{con}	Conduction current
I	Terminal current
I_{DIS}	Displacement current
I_{DIF}	Diffusion current
I_g	Gate current
I_D	Drain current
I_S	Source current
J	Conduction current density
J_{tot}	Total current density
j_D	Displacement current density
j_{DIF}	Diffusion current density
k	Boltzmann's constant

LIST OF SYMBOLS
(continued)

l_g	Gate length
N_D	Donor impurity concentration
n	Charge carrier concentration
q	Electron Charge
R	Resistance
T	Absolute temperature
t	time
v	charge carrier velocity
v_s	charge carrier saturated velocity
V_{DS}	Drain to source voltage
V_{SG}	Source to gate voltage
V_P	Pinchoff voltage
W	MESFET width
ϵ_r	Dielectric constant
ϵ_0	Vacuum dielectric permittivity
$\epsilon = \epsilon_0 \epsilon_r$	Dielectric permittivity
λ_D	Debye length
μ_0	Low-field mobility
σ	Conductivity
ϕ_B	Built-in potential of the Schottky barrier
ψ	Electric potential

1. FET ANALYSIS METHODS

1.1 INTRODUCTION

As suggested by the title, this report presents a novel practical AC large-signal model for the GaAs MESFET. The new model is a "true" AC large signal one in the sense that the total terminal currents are given as explicit functions of the total terminal voltages V_{SG} , V_{DS} , and their time derivatives. Previous models and simulations were either DC alone, or a DC analysis with a small-signal incremental AC model derived from it. Few authors attempted "true" AC simulation by numerical time-dependent solution to the device differential equations. This approach is ordinarily very expensive and extremely time-consuming on a digital computer.

The present model is circuit design oriented and can be used to analyze and design large-signal components (oscillators, power amplifiers, frequency multipliers, etc.). As such it is very efficient and fast on a digital computer. To achieve this an approximate analytic solution

to the device differential equations was derived. Since the model is derived from basic principles, it is directly dependent on device geometry and the semiconductor properties.

Our analysis is based on the general method suggested by Yamaguchi and Kodera [1]*. Their basic approach was extended and improved in two ways: 1) by extending it into a "true" AC large signal model 2) by making it almost completely analytic by solving for an unknown parameter in their equations in an analytic fashion instead of their numerical iterative method. This improves dramatically the computation time, which is 0.05-0.1 seconds per point in our model compared to 1 second for the iterative method. The model has only modest memory requirements (50K words on IBM 360).

This chapter includes a review of the main FET analysis methods presented in the literature. The review starts with the classical Shockley approach and ends with the more recent modern approaches. The various advantages, disadvantages and limitation of each method are discussed. Special attention is given to the validity of the analysis methods for modern high-frequency GaAs devices. These devices are characterized by very short gates (micron or

* The numbers in parenthesis in the text indicate references in the Bibliography.

sub-micron), thus yielding relatively small length to height ratios for which the Shockley gradual approximation may be invalid. Also, the electric field in the device is normally very high, thus making the device properties dominated by saturation of the velocity of the charge carriers.

1.2 SHOCKLEY MODEL

The so-called field-effect transistor was first introduced by Shockley [2] in 1952. Shockley suggested the construction of the new device and developed a detailed analysis of it. This was basically a DC analysis, and as a result the I-V curves of the new device were deduced.

Shockley also derived a simplified incremental small signal AC model. The basic limitations of this analysis are:

- 1) charge carriers are assumed to have constant mobility - no consideration of velocity saturation.
 - 2) one dimensional approach - only one component of the electric field is considered (the quadrature component is assumed zero).
 - 3) abrupt transition assumed between the conducting channel and the depletion region.
- To avoid confusion in the review of Shockley's model below, his notation is used.

1.2.1 Device Structure And Basic Properties

The device introduced by Shockley is illustrated in Figure 1-1. It is a three-terminal device consisting of a p-type layer sandwiched between two layers of n^+ type material. The electric current is composed of holes flowing

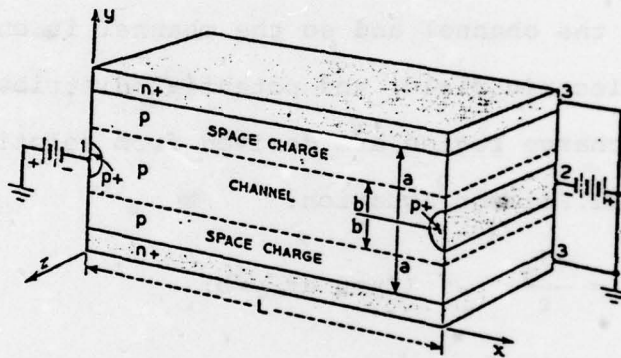


Figure 1.1 FET structure (after Shockley [2])

in the x-direction in the p layer. The terminal contacts are formed by p^+ material. In normal operation reverse bias is applied to the two junctions, which form the space-charge regions in which the carrier concentration is practically zero. So the carriers flow in a channel of p-type material bounded by two space-charge regions.

As a first step assume that the applied voltages across the two junctions are equal. This means that no current is in the channel and so the channel is uniform. The charge, electric field, and potential distributions in the space charge region are derived from solution to the one dimensional Poisson Equation:

$$\frac{dEy}{dy} = \frac{qN_a}{\epsilon} \quad (Ey=0 \text{ at } y=b) \quad (1-1)$$

which yields:

$$Ey = - \frac{qN_a}{\epsilon} (y-b) \quad (1-2)$$

$$V = \frac{qN_a}{2\epsilon} [(y-b)^2 - (a-b)^2] \quad (1-3)$$

The constant of integration was chosen to make $V=0$ at $y=a$ (gate as the reference voltage).

The potential in the channel is:

$$V(y=b) = - \frac{qN_a}{2\epsilon} (a-b)^2 \quad (1-4)$$

To avoid using negative numbers in the derivation, Shockley defined:

$$W = - V(y=b) = [1-(b/a)]^2 W_0 \quad (1-5)$$

$$W_0 = \frac{qN_a}{2\epsilon} a^2 \quad (1-6)$$

W_0 is the voltage required to make the space charge penetrate the entire p-region. He termed this as the "pinch-off" voltage.

Now assume there is a small difference between the voltages applied across the two junctions. In that case the channel can be assumed almost uniform as before. The channel conductivity is $qN_a\mu_0$, where μ_0 is the hole mobility (assumed constant). Thus, the current per unit width in the channel for an applied E_x is:

$$I = 2bqN_a\mu_0 E_x = g(W) E_x \quad (1-7)$$

$$g(W) = 2qN_a\mu_0 b \quad (1-8)$$

$g(W)$ is the conductance of a unit square of the layer $2b$ thick. So, the total conductance per unit width is

$$G = g(W)/L \quad (1-9)$$

$g(W)$ is a function of the reverse bias W . Using Equations 1-9, 1-5 one gets:

$$g(W) = [1 - \left(\frac{W}{W_0}\right)^{1/2}] g_0 \quad (1-10)$$

where $g_0 = 2qN_a\mu_0 a$

Equation 1-10 clearly demonstrates the basic principle of FET operation, namely, a voltage controlled conductance.

Shockley suggested the following names to the electrodes:

source for electrode 1 through which the carriers flow into the channel.

drain for electrode 2 through which the carriers flow out of the channel.

gate for the control electrode 3.

These names were accepted and are commonly used.

1.2.2 The Gradual Case

When the applied source and drain voltages are not equal the channel is not uniform, and Equation 1-5 is invalid, since it was derived for the one-dimensional case. However, if $\frac{\partial^2 V}{\partial x^2}$ in the depletion region is very small compared to qNa/ϵ , then the one dimensional approximation is valid and so is Equation 1-5. For the above to be true the conditions along the channel should vary gradually, thus this assumption is called by Shockley the "gradual approximation". The gradual approximation holds if $\frac{db}{dx} \ll 1$. In the gradual case the electric field in the space charge region is assumed to be in the y direction, while in the channel it is assumed to be in the x direction.

The basic equation for the gradual case is:

$$I = g(W) \frac{dW}{dx} \quad (1-11)$$

which is equivalent to Equation 1-7.

Rearrange and integrate Equation 1-11 and get:

$$I \int_0^L dx = \int_{W_s}^{W_d} g(W) dW \quad (1-12)$$

$$I = \frac{1}{L} \int_{W_s}^{W_d} g(W) dW \quad (1-13)$$

Define the function:

$$J(W) = \int_0^W g(W) dW = g_0 W \left[1 - \frac{2}{3} \left(\frac{W}{W_0} \right)^{1/2} \right] \quad (1-14)$$

Then:

$$\begin{aligned} I &= [J(W_d) - J(W_s)]/L \\ &= [J(V_g - V_d) - J(V_g - V_s)]/L \end{aligned} \quad (1-15)$$

A plot of I vs. $|V_d|$ with V_g as a parameter and $V_s = 0$ is given in Figure 1-2. Equation 1-15 is not valid for $W_d > W_0$ because pinchoff occurs and the gradual approximation fails. The continuation of the curves in Figure 1-2 is based on the analysis developed in the next section. The critical condition for pinchoff ($W_d = W_0$) is indicated by the dashed line. The equation for this curve is

$$I = [J(W_0) - J(W_0 - |V_d|)]/L \quad (1-16)$$

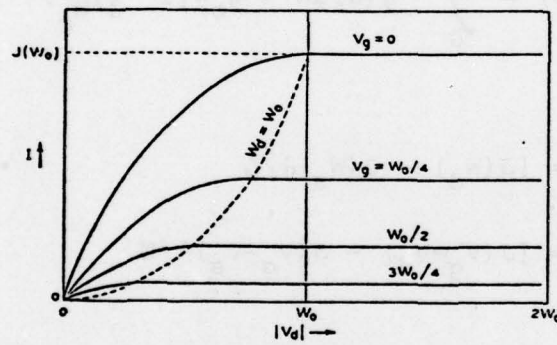


Figure 1.2 Current-voltage characteristics for FET (after Shockley [2])

In the case of a small-signal AC superimposed on the DC it is possible to calculate the small signal drain current as a function of the small signal voltage by taking the time derivative of Equation 1-15. The result is:

$$i_d = -i = G_{dg}[(v_g - v_s) + (v_d - v_g)/\mu_{dg}] \quad (1-17)$$

where:

$$G_{dg} = g(W_s)/L \quad (1-18)$$

$$R_d = L/g(W_d) \quad (1-19)$$

$$\mu_{dg} = G_{dg} R_d \quad (1-20)$$

Equation 1-17 suggests a small signal AC equivalent circuit for the FET as shown in Figure 1-3. This is an over-simplified equivalent circuit and does not include any parasitic elements.

Shockley also derives the channel shape (i.e. b vs. X). From Equation 1-5

$$dW = \frac{-(a-b)qN_a}{\epsilon} db \quad (1-21)$$

and insertion into Equation 1-11 leads to

$$IdX = -I_o a(1-u)u du \quad (1-22)$$

where:

$$u \equiv b/a \quad (1-23)$$

$$I_o = g_o E_o \quad (1-24)$$

$$E_o = 2W_o/a \quad (1-25)$$

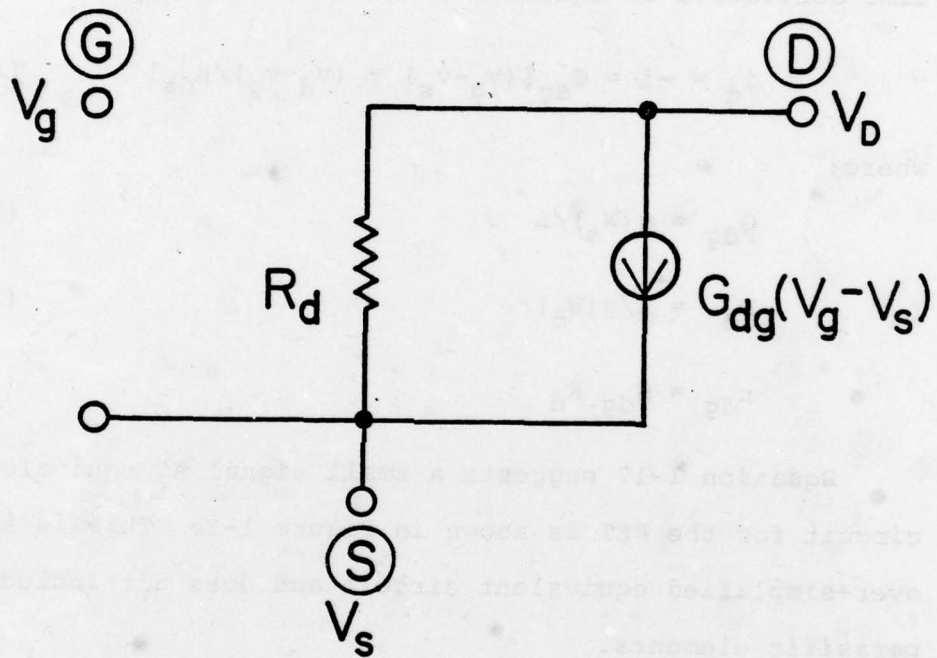


Figure 1.3 Shockley's small signal equivalent network for FET

Integrating Equation 1-22 yields

$$x = - \left(\frac{aI_0}{I} \right) \left[\frac{u^2}{2} - \frac{u^3}{3} \right] \quad (1-26)$$

Equation 1-26 gives the shape of the channel. Once it is known the voltage along the channel is readily calculated using Equation 1-5.

Using Equation 1-26 it is possible to derive the condition for the validity of the gradual approximation: over a distance a the fractional change in channel width is small:

$$\frac{a}{b} \frac{db}{dx} = \frac{I}{(1-u)u^2 I_0} < 1 \quad (1-27)$$

From the above equation it is obvious that the gradual approximation fails for $u=0$ and $u=1$. For $u=1$ (full channel) the failure is of little importance since the electric field is small and the conductance large. Also $u=1$ does not happen in practice, since there is always some residual depletion region. For $u=0$ the electric field is high, and this case is always approached when $W_d > W_0$. For $u \rightarrow 0$ Equation 1-27 becomes:

$$\frac{I}{u^2 I_0} < 1 \quad (1-28)$$

Also Equation 1-26 becomes:

$$-x = \frac{I_0 a u^2}{2I} \quad (1-29)$$

Combining them one obtains:

$$-x > \frac{a}{2} \quad (1-30)$$

So, the gradual approximation holds at distances greater than $a/2$ away from the end of the channel (the point $u=0$). Therefore, the complete disappearance of the channel as predicted by Equation 1-26 does not occur. However, it is convenient to define the extrapolated pinchoff point (expop) as the point at which the channel would vanish and W would equal to W_0 if the gradual solution was continued beyond its range of validity.

1.2.3 The Expop Region

When $W_d > W_0$ an expop exists in the channel somewhere between source and drain. If the gradual approximation would hold the channel would have been pinched off, and between the expop and the drain there would be no channel. In practice, the channel tends to vanish near the expop, but the charge carriers "push" their way and form a narrow constriction at $y=0$. Since the charge due to these holes is very small compared to the space charge in the depletion region, that part of the electrostatic potential which is due to charges is well approximated by

$$V_0(x,y) = -W_0 \left[1 - \left(\frac{y}{a} \right)^2 \right] \quad (1-31)$$

which satisfied Poisson's equation and goes to zero at $y = \pm a$ and to $-W_0$ at $y=0$. This potential is independent

of X and produces no field which causes the holes to flow. The field E_x is produced by the drain voltage. The potential distribution due to drain voltage is the solution of Laplace's equation with the boundary condition that it vanishes at $y = \pm a$. The general solution is:

$$T(x,y) = \sum_{n=0}^{\infty} A_n \exp[\pi(2n+1)X/2a] \cos[\pi(2n+1)y/2a] \quad (1-32)$$

The zero order term ($n=0$) is usually an adequate approximation to the potential function, due to the exponential decay (the decay per each interval of a is $e^{-\pi/2} = 0.21$ for $n=0$, and $e^{-\frac{3\pi}{2}} = 0.009$ for $n=1$). So, in the vicinity of the expop the potential is approximated by

$$V(x,y) = V_0(x,y) - AT_0(x,y) \quad (1-33)$$

where $V_0(x,y)$ is given by Equation 1-31 and:

$$T_0(x,y) = \exp(\pi X/2a) \cos(\pi y/2a) \quad (1-34)$$

The only problem left is to determine the coefficient A . Shockley determines it by a graphical method. He draws a graph of the potential versus X . For $x < -\frac{a}{2}$ he uses Equations 1-26 and 1-5. For $X > a$, Equation 1-33 is used with several values of A . By observing the graphs (Figure 12 in [2]), Shockley chose that value for A , which gave a "smooth" transition from the gradual to the exponential solution. This value of A is

$$A = W_o \left(\frac{I}{2I_o} \right)^{1/2} \quad (1-35)$$

Using Equation 1-33 for the drain $V(X_d) = -W_d$ it is possible to solve for X_d , the distance between the drain and expop:

$$X_d = \frac{2a}{\pi} \ln [(W_d - W_o) (2I_o/I)^{1/2} / W_o] \quad (1-36)$$

The logarithmic dependence of X_d on drain voltage and current suggests that X_d is insensitive to these values. As an example, for $I_o/I = 18$, X_d changes from 1.15a at $W_d = 2W_o$ to 2a at $W_d = 5W_o$. In view of the above it is possible to explain the continuation of the curves in Figure 1-2 for $|V_d| > W_o$. Equation 1-11 holds only for the gradual portion of the channel, and the integration must be taken between W_s and W_o . Accordingly, X varies from zero to a distance L_s up to the expop, where:

$$L_s = L - X_d \quad (1-37)$$

The result of the integration is

$$I = [J(W_o) - J(V_g - V_s)] / L_s \quad (1-38)$$

Therefore, for $W_d > W_o$ the current is almost independent of V_d , thus explaining the horizontal line continuation in Figure 1-2. There is a weak dependence on V_d via L_s . In fact, as $|V_d|$ increases, X_d increases, L_s decreases,

and I increases. Thus, the curves are not horizontal but have a slight positive slope.

The corresponding small signal AC equation can be derived in a way similar to that in the previous section. Starting with equation:

$$I(L - X_d) = \int_{W_s}^{W_o} g(W) dW \quad (1-39)$$

take appropriate derivatives and get:

$$i = I \left[\frac{v_s}{E_{xs}} - \frac{v_d}{E_{xd}} + v_g \left(\frac{1}{E_{xd}} - \frac{1}{E_{xs}} \right) \right] / (L - X_d + \frac{a}{\pi}) \quad (1-40)$$

where:

$$E_{xs} = I/g(W_s) \quad (1-41)$$

$$E_{xd} = \frac{\pi}{2a} (W_d - W_o) \quad (1-42)$$

Comparing Equation 1-40 to Equation 1-17 one can conclude:

$$\mu_{dg} = \frac{E_{xd}}{E_{xs}} - 1 \quad (1-43)$$

$$G_{dg} = \frac{\mu_{dg} g(W_s)}{(L - X_d + \frac{a}{\pi}) (1 + \mu_{dg})} \quad (1-44)$$

$$R_d = \frac{1}{G_{dg} \mu_{dg}} \quad (1-45)$$

So, the equivalent circuit is the same as in Figure 1-3 but the component values are calculated from Equations 1-43 to 1-45.

1.2.4 Discussion

The Shockley equations as derived above are generally valid and useful for low frequency devices. These are usually made of silicon or germanium, their gate length is typically several microns, and their thickness is large compared to Debye length:

$$\lambda_D = \sqrt{\frac{\epsilon kT}{q^2 N_D}} \quad (1-46)$$

Under these conditions the electric field in the device is low enough so that no velocity saturation exists. Also, the transition region between the channel and the depletion region (which is in the order of a Debye length) is negligible, so that an abrupt transition assumption is reasonable. Also, since the device length to height ratio is large, the gradual approximation holds and a one dimensional approach is acceptable.

Modern high frequency devices are made of GaAs or InP materials with low threshold field for velocity saturation. The gate length is on the order of 1 μm and even less, and the height is usually less than 0.5 μm . For these devices the electric field is usually much higher than the threshold for velocity saturation, thus the device properties are strongly affected by velocity saturation effects. Also, the length to height ratio is not large, so the gradual approximation is generally invalid, and a two-

dimensional approach is necessary. Also, since the device height is not very large compared to the Debye length, it is necessary to take into account a non-zero transition region between the channel and the depletion region.

In addition to the above, for the high frequency devices it is necessary to calculate the displacement currents and the capacitive effects associated with them, as well as other high frequency effects such as transit time through the device and a depletion region charging time constant. Shockley did not consider these effects.

In the last decade, when the advantages of the FET for high frequencies were realized, many researchers faced the problem of a lack of a valid model for the high frequency FET. Therefore, much work has been done during the last few years to develop a useful model. The next paragraphs of this chapter contain descriptions of these efforts, as well as their advantages and disadvantages.

1.3 MODERN ANALYSIS METHODS

1.3.1 High Frequency FET Structure

The modern high frequency FETs are constructed in a different way than the low frequency devices proposed by Shockley (Figure 1-1). They are usually fabricated in a planar structure as shown in Figure 1-4. The device is built on a semi-insulating substrate (GaAs or InP). On top of this substrate an epitaxial layer of n-type material

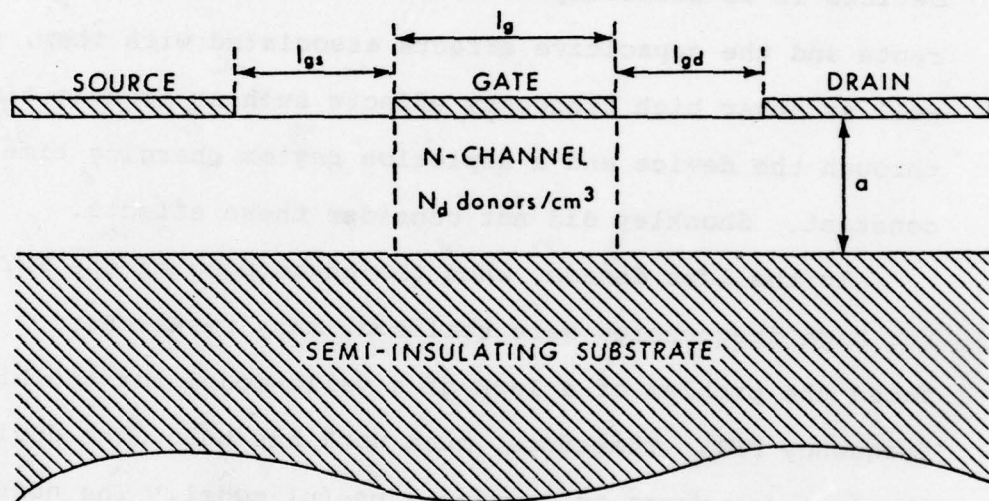


Figure 1.4 Typical high frequency FET structure

is grown. A typical doping level is 10^{17} cm^{-3} . The electrode metalization is deposited on top of the epitaxial layer, thus achieving a planar device which is easier to process compared to the Shockley structure. Note, that the device in Figure 1-4 is not symmetrical as in the Shockley device (only one gate electrode). Also it has a Schottky-barrier junction rather than the p-n junction in the Shockley device. The high frequency devices are always n-channel to utilize the much higher mobility of electrons compared to holes. Although most of the modern analysis methods described below refer to the high frequency structure (Figure 1-4), they are equally applicable to the Shockley device.

1.3.2 General Approaches

Some of the important papers dealing with high frequency FET modeling are listed in the reference list ([1], [3]-[21]). Before describing the special features of some of these models it is useful to present the general approaches used by the authors. The various simulations belong in one of two major categories: a) extension and correction of Shockley model. b) numerical solution to the device differential equations. References [9], [17] do not belong to either of the above approaches. They deal with special methods to be described below.

References [3],[4],[6],[8],[10],[12],[13],[18] use approach (a), that is, they try to improve Shockley's model and adapt it to high-frequency devices. The general characteristics of these methods are:

- 1) basically a one dimensional approach (with some two dimensional analysis for the high field region like Shockley).

- 2) assumption of an abrupt transition from channel to depletion region.

- 3) incorporation of velocity saturation effects on the I-V curve (basically follow Turner and Wilson [3] approach).

- 4) extension of Shockley's analysis for the high field drain region.

From this group of papers the basic paper of Turner and Wilson [3] is discussed in some detail later in this chapter.

References [1],[5],[7],[11],[14]-[16],[19]-[21] use approach (b), namely, a numerical solution to the device differential equations. The characteristics of this approach are:

- 1) Start from basic principles and write the exact partial differential equations describing the device behavior (two-dimensional).

- 2) State the boundary conditions applicable to the geometric structure.

3) Solve the equations under the stated boundary conditions.

Since the above equations are usually quite complicated, no analytic solution has been published, and it seems unlikely that such a solution will be found. However, with existing powerful digital computers and the advanced state of numerical analysis it is quite feasible to solve the equations numerically. This has been done quite extensively in the last few years, thus yielding accurate characterization of FETs. Since no major assumption or approximation is done in formulating the equations, the simulation is accurate (provided, of course, a good and stable numerical method is employed). The greatest disadvantage of this approach is the large computation time (and large expense associated with it). The new model to be described in this report removes this disadvantage.

The FET differential equations are (see, for example, Yamaguchi and Koderia [1], Kennedy and O'Brien [5] or Reiser [7]):

$$\nabla^2 \psi = -\frac{q}{\epsilon} (N_D - n) \quad (1-47)$$

$$q \frac{\partial n}{\partial t} = \nabla \cdot \bar{J} \quad (1-48)$$

$$\bar{J} = -qn \bar{V} + qD \nabla n \quad (1-49)$$

$$\bar{J}_{\text{tot}} = \bar{J} + \epsilon \frac{\partial \bar{E}}{\partial t} \quad (1-50)$$

Equation 1-47 is Poisson's equation, Equation 1-48 is the current continuity equation, Equation 1-49 defines the conduction current (drift and diffusion), and Equation 1-50 defines the total current (conduction and displacement).

The numerical solution to the above equations is performed using the following steps:

- 1) define a grid of points in the two dimensional region.
- 2) approximate derivatives by differences.
- 3) use (2) in the above equations for each point of the grid.
- 4) get a set of linear algebraic equations
(the number of equations is equal to the number of grid points).
- 5) solve the above set using standard computer sub-routines.

Some of the important results reported in the literature using this approach are described in the following sections.

1.3.3 Turner And Wilson Model

A good example of an approach attempting to correct the classical Shockley model is the Turner and Wilson model [3]. Many of the recent publications are basically an improvement of this model. The main contribution reported

in [3] is the incorporation of velocity saturation effects on device properties. Although Turner and Wilson consider the non-symmetrical device (Figure 1-4), the analysis is applicable to the Shockley device too.

The basic idea is to use the Shockley equations for low V_{DS} , where the electric field is below the critical field for velocity saturation. At the onset of velocity saturation the current through the device can be expressed both using the Shockley expression and also as:

$$I_m = I_o (1-u) \quad (1-51)$$

$$I_o = qN_D v_s W a \quad (1-52)$$

where

$$u^2 = (V_{DS} - V_{GS})/V_P$$

Equating the two expressions gives an equation for u at the onset of velocity saturation:

$$\frac{3E_c l g}{V_P} = \frac{3u^2 - 2u^3}{1-u} \quad (1-53)$$

Thus the I-V curves of the device are calculated by using the Shockley equation from $V_{DS} = 0$ to the point determined by the critical u , at which point the current

remains constant (independent of V_{DS}). This is demonstrated in Figure 3 of [3]. As argued in the Shockley model, here too the current does not actually remain constant, but has a slight positive slope. Beside the correction to the I-V curve, Turner and Wilson also derive corrections to the transconductance and input capacitance as function of the parameter u . For $V_{gs} = 0$ the equations are:

$$g_m = g_{mo} \frac{(3-2u)u}{6-9u+4u^2} \quad (1-54)$$

$$C_{in} = \frac{3\epsilon W l g}{a} \frac{36-84u+67u^2-18u^3}{u(3-2u)^2(6-9u+4u^2)} \quad (1-55)$$

g_{mo} is the transconductance calculated by Shockley's equation.

This model has the same basic limitations as the Shockley model, except that the effect of velocity saturation on some of the device properties is considered.

1.3.4 Kennedy And O'Brien Simulations

One of the first attempts to solve the FET differential equations numerically, and thus predict the device behavior, was made by Kennedy and O'Brien [5]. They present an extensive amount of data generated by the computer simulation. Some of their important results are described below. All their simulations are done for silicon devices, thus avoiding the negative differential

mobility of GaAs with the charge accumulation accompanying it. The device analyzed is similar to Shockley's structure (Figure 1-1).

The data are presented in three types of Figures: map of charge carriers distribution, map of electric potential distribution, and I_D vs. V_{DS} curve with V_{sg} constant. The authors compare their data to data derived from Shockley's equations and also check some of Shockley's assumptions.

The important observations and conclusions are:

- 1) The transition from the neutral channel to the depletion region is gradual and not abrupt as Shockley assumed. There exists a very clear transition region, which may be important for thin devices.

- 2) In the case of field-dependent mobility, namely, velocity saturation, there is some charge accumulation in the device in the high field region near the drain, accompanied with a depletion region further toward the drain to preserve charge neutrality. The explanation suggested by the authors to this phenomenon is simply current continuity in the device. Toward the drain the channel narrows. In the case of constant mobility the current is kept constant by the increase in electric field. However, when the velocity is saturated, the only way to keep the current constant in spite of the narrowing channel is by charge accumulation. It is worthwhile mentioning here that there is another mechanism to keep the current

constant. Since the problem is two-dimensional, the velocity vector can rotate. Thus the x component of the velocity can increase inspite of the fact that the magnitude of the velocity vector is constant. This mechanism was suggested by Yamaguchi and Kodera [1] and is discussed further in this chapter.

3) In the case of velocity saturation the drain current vs. V_{DS} curve saturates for voltages below the Shockley "pinchoff voltage". Thus, the main reason for current saturation is the charge carrier velocity saturation and not pinchoff effects. In fact, by observing Kennedy and O'Brien's charge distribution maps it is seen that for many devices the channel is never pinched off even for very large V_{DS} .

4) By observing the electric potential maps one concludes that the one dimensional approach of Shockley is not valid for gate length to epitaxial layer thickness ratio smaller than 5. Even when the ratio is 5 the constant potential contours are not parallel to the device axes, thus suggesting that the electric field is two-dimensional.

Thus, the extensive computer simulations of Kennedy and O'Brien yield useful data which help in the understanding of some of the physical properties of the FET. These simulations are also very useful for checking the

approximations made by many authors. Since 1970 much more work has been done on numerical simulations, including those for GaAs devices. Some of this work is described in the next three sections.

1.3.5 Barnes' Simulations

One of the recent extensive numerical simulations of a GaAs MESFET was performed by Barnes [14]. Like most of the previous simulations this one is based on the numerical solution of the partial differential equations of the device. The report contains a large number of graphs displaying the calculated characteristics of several devices. The author uses three dimensional graphics to display functions like charge carrier concentration, voltage, electric field etc. vs. both x and y (as an example, see Figure 1-5).

Most of the data generated is for DC conditions, thus allowing the calculation of the static I-V curves. The author uses his simulation program to investigate the physical properties of the device and their dependence on various parameters such as doping level, geometry, non-uniform doping, substrate effects, etc. It is worthwhile noting that the simulations are performed for doping levels in the range 10^{15} - 10^{16} cm^{-3} . No simulation is presented for more practical devices in the range 10^{17} cm^{-3} . The reason for this is probably the much larger number of grid

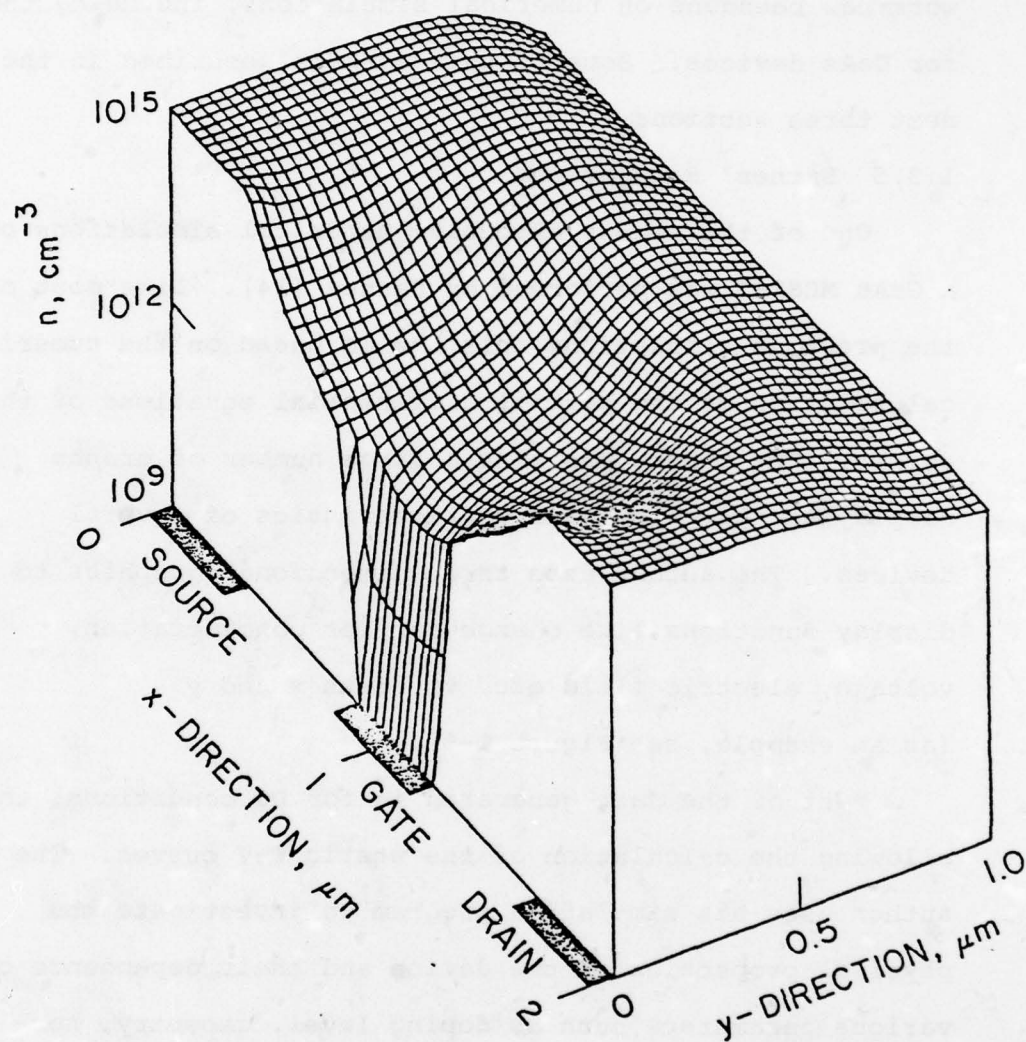


Figure 1.5 A three dimensional graph of electron distribution (after Barnes [14])

points necessary in the high doping case to obtain a stable numerical solution. Obviously, when the number of grid points is too large the simulation is not practical due to both excessive memory requirements and extremely large computation time.

Barnes' simulation is a good example of the usefulness of numerical methods for the purpose of FET investigation. Although it is expensive and time consuming, the data generated is accurate, and useful in the understanding of the device properties.

1.3.6 Yamaguchi And Koderia Simulations

Another interesting simulation is the one developed by Yamaguchi and Koderia [1] and its extension with S. Asai [15]. Paper [1] serves also as the basis for the practical model described in this thesis. This aspect is presented in detail in chapter 2. Here only some results of their numerical simulation are presented. The simulation in [1] neglects the negative differential mobility of GaAs, and the assumption is made that:

$$v(E) = \begin{cases} \mu_o E & \text{for } E \leq E \text{ critical} \\ v_s & \text{for } E > E \text{ critical} \end{cases} \quad (1-56)$$

Some results of the numerical simulation are given in the form of charge-carrier density plots, I-V curves, etc. An interesting result emerging from their simulation is an

explanation of current mechanism in the device for the case of carrier velocity saturation on the drain side, but no saturation on the source side. Kennedy and O'Brien [5] have already shown that to maintain current continuity there is a possibility of charge accumulation on the drain side. Yamaguchi and Koderá have pointed out another mechanism: rotation of the velocity vector. Even though the velocity is constant at v_s on the drain side, as V_{DS} increases the velocity vector rotates such as to increase the longitudinal component of the velocity. This increases the drain current. In practice both mechanism exist. For thick devices (compared to about 6 times Debye length) the charge accumulation effect is dominant, while for thin devices the velocity vector rotation is dominant.

The aspect of instability in FETs due to Gunn domain formation is analyzed in [15]. As in [1] here too a numerical simulation is performed, however, here the negative differential mobility is considered. Generally, the simulation shows that instability is possible in relatively thick devices. The simulation actually shows the formation of a domain traveling from gate to drain. As the device is made thinner the traveling domain becomes a static domain (appreciable charge accumulation near the drain). For even thinner devices the domain disappears, and the device properties are practically like those of a

silicon device (the authors call this a "pentode-like" operation). Based on their numerical analysis, the authors developed an approximate analytic criterion for determining the stability of a given device. Define:

$$W_{th} = \left\{ \frac{2\epsilon}{qN_D} (\phi_B + V_{SG} + E_{th} \lg) \right\}^{1/2} \quad (1-57)$$

where: ϕ_B - built in potential of the Schottky barrier junction.

E_{th} - critical field for negative differential mobility.

V_{SG} - source to gate voltage.

The device is absolutely stable (no Gunn domains) if the device thickness is less than W_{th} . For device thicknesses between W_{th} and $2W_{th}$ a static domain exists (this shows up in the I-V curves as a negative resistance region). For device thicknesses over $2W_{th}$, travelling domain exists.

The above criterion is very useful and enables the design of stable devices. It also sets limits on the validity of simulations which neglect the negative differential mobility of GaAs.

Shur and Eastman [22] have attempted to improve the original Yamaguchi and Koder model [1] by considering a static domain. They have subdivided the device into two

regions: 1) under the gate - simulated by the Yamaguchi and Koderia model; and 2) gate to drain region - simulated by a static domain. There is some inaccuracy involved in this assumption since usually the domain penetrates substantially into the gate region.

1.3.7 Grubin And McHugh Simulations

An interesting numerical analysis was presented by Grubin [16] and Grubin and McHugh ([20],[21]). The emphasis in their simulation is the investigation of the instabilities due to Gunn domain formation. The analysis is a "true" time dependent AC large signal analysis. The problem is three dimensional (two spatial coordinates and time). As mentioned above numerical simulation of this type is time consuming and expensive. To reduce time and cost the analysis was made for 10^{15} cm^{-3} doping level (instead of the realistic value around 10^{17} cm^{-3}), thus requiring many fewer grid points for the numerical analysis.

The analysis performed is of the transient response type. The gate to source and drain to source voltages are changed rapidly from one DC value to another, and the transient response in current, voltage and charge is observed. For "thin" devices the transient response is normal, in the sense that the charge in the device was rearranged to accomodate the new DC conditions, and this was done gradually according to the appropriate time constant. However, for "thick" devices, the DC bias change

triggered the formation for Gunn domains, and oscillations were observed. A travelling domain exists between gate and drain. The analysis shows that for each potentially unstable device there is a range of DC conditions in which the device is unstable, but if the drain to source voltage is increased or decreased to bring the device outside of this region, the oscillation stops.

1.3.8 Semi-Empirical Analysis

As mentioned above, the numerical simulations are accurate and useful but impractical for circuit design. A semi-empirical approach to achieve a circuit design oriented simulation was developed by Willing and Rauscher [17]. Their approach is pursued as follows:

1. Stipulate an equivalent circuit for the FET containing several fixed elements and some bias-sensitive (non-linear) elements. Willing and Rauscher chose a topology similar to the commonly used small signal equivalent circuit (see [17]).
2. Measure the small-signal s-parameters of the device for the full bias range required.
3. Calculate the fixed and bias sensitive elements of the equivalent circuit by curve fitting the measured and calculated small-signal s-parameters, thus getting the full quantitative representation of the device.

Large signal analysis is performed by embedding the above equivalent circuit in the complete network to be analyzed and solving the network time-domain differential equations.

The advantage of the above approach is its efficiency and low cost (once the equivalent circuit is known). The disadvantages are: 1) a long and costly process of measurements to establish the equivalent circuit for each device; and 2) no direct dependence on device geometry and other properties, since this is a phenomenological approach, and is not based on first principles.

1.4 SCOPE OF THIS REPORT

As mentioned in the beginning of this chapter it is devoted to a review of the main FET analysis methods published in the literature. The rest of the report includes the following topics:

Chapter 2 develops the basic analysis approach employed in the new model as suggested by Yamaguchi and Koderia [1]. Chapter 3 includes the actual derivations for the gate-region analytic model. Emphasized are the improvements made to make the model "true AC". The complete FET model (including internal and external parasitics) is presented in chapter 4. The application of the model is illustrated in chapter 5. The data generated

by the model are presented in graphical form, and include static properties, s-parameters, waveforms, harmonic distortion, etc. Chapter 6 contains conclusions and suggestions for future work.

2. THE BASIC APPROXIMATE ANALYTIC SOLUTION

2.1 INTRODUCTION

The fundamental ideas and derivations upon which the present FET model is based are presented in this chapter. First outlined is the basic approach of Yamaguchi and Koderia [1]. The idea of postulating a "reasonable" functional behaviour for the charge carrier concentration is explained, and the derivation of the resulting parametric analytic solution is presented. The analytic determination of the parameter, which is one of the improvements reported here, is derived in chapter 3.

Once the parameter is known, the problem is solved and the electric field and charge carrier density can be calculated. Thus, by calculating the current density and integrating over the proper electrodes, the drain, source and gate currents can be calculated. These are the total currents (conduction and displacement), and thus depend on the terminal voltages and their time derivatives. The expressions for the currents are derived in this chapter. Also, from the displacement current expressions, the small signal input and output capacitances are computed as functions of the DC bias voltages.

2.2 PROBLEM DEFINITION

The device analysed in this report has a structure as presented in Figure 1-4, namely it is a planar structure,

with the three electrodes deposited on top of the epitaxial layer. The source and drain electrodes form an ohmic contact, while the gate electrode forms a Schottky barrier junction. The semi-insulating substrate is considered a perfect insulator. Of course, it is possible to account for substrate losses by an external effective resistor between the source and drain contacts.

For simplicity, only the active region directly under the gate is considered in the analysis. The effect of the two regions outside the gate electrode (source-gate and gate-drain spacings) is considered in chapter 4. Therefore, the geometrical structure to be analysed is as given in Figure 2-1. The source reference point is (0,0). At this point the potential is taken as zero. The drain point is at (lg, 0), and the potential there is assumed V_{DS} (a given boundary condition). The gate extends from $x=0$ to $x=lg$ at $y=a$. The potential at the gate is $-(\phi_B + V_{SG})$, where ϕ_B is the built-in potential of the Schottky barrier junction and V_{SG} is a given boundary condition. The differential equations to be solved are (1-47) to (1-50), which are reproduced here for convenience:

$$\nabla^2 \psi = -\frac{q}{\epsilon} (N_D - n) \quad (2-1)$$

$$q \frac{\partial n}{\partial t} = \nabla \cdot \bar{J} \quad (2-2)$$

$$\bar{J} = -qn\bar{V} + qD\nabla n \quad (2-3)$$

$$\bar{J}_{tot} = \bar{J} + \epsilon \frac{\partial \bar{E}}{\partial t} \quad (2-4)$$

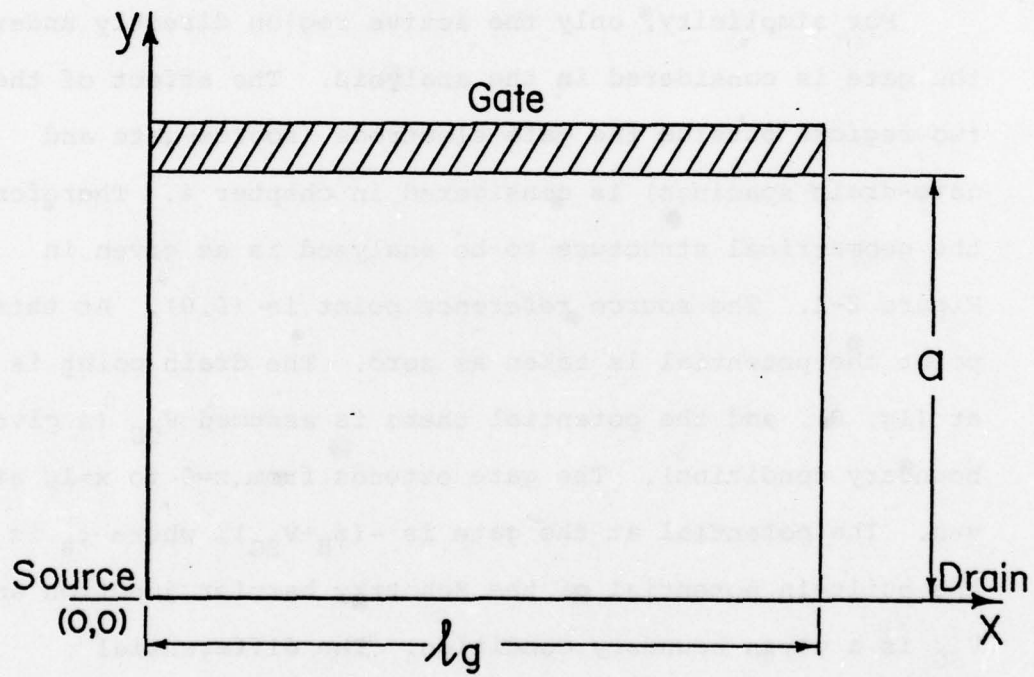


Figure 2.1 Gate active region considered in the analysis

The above equations represent two coupled partial differential equations in the variables ψ , n . The boundary conditions are:

$$\psi(0,0) = 0 \quad (2-5)$$

$$\psi(x,a) = -(\phi_B + V_{SG}) \quad (2-6)$$

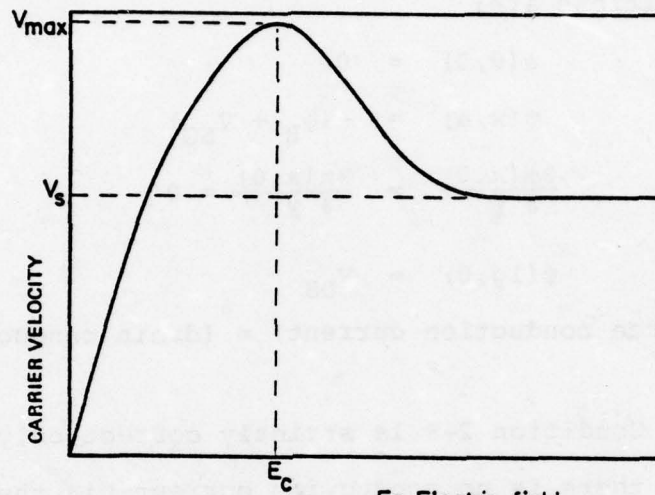
$$\frac{\partial \psi(x,0)}{\partial y} = \frac{\partial n(x,0)}{\partial y} = 0 \quad (2-7)$$

$$\psi(lg,0) = V_{DS} \quad (2-8)$$

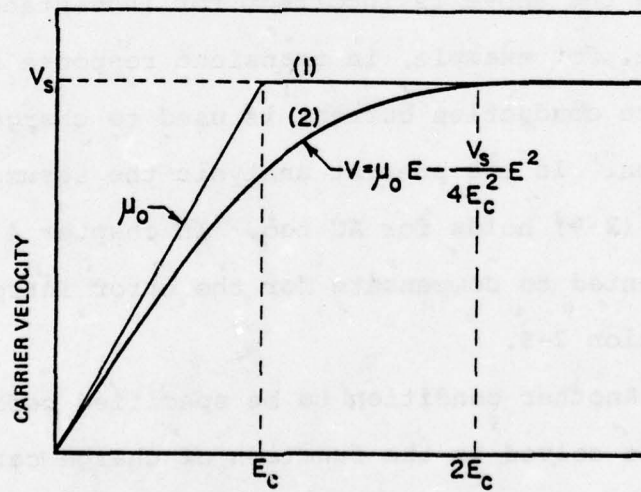
$$(\text{source conduction current}) = (\text{drain conduction current}) \quad (2-9)$$

Condition 2-9 is strictly correct only for DC since then there is no conduction current via the gate. For AC drive the above is incorrect for instantaneous currents since, for example, in transient response some of the source conduction current is used to charge the depletion region. In the present analysis the assumption is made that (2-9) holds for AC too. In chapter 4 a method is presented to compensate for the error introduced by using Equation 2-9.

Another condition to be specified before the equations can be solved is the function of charge carrier velocity versus electric field. This function is a property of the material. Figure 2-2(a) presents the velocity field relation for GaAs. Typical values are: $E_c = 3.2 \text{ KV/cm}$, $v_s = 10^7 \text{ cm/sec}$, $v_{\max} = 2 \cdot 10^7 \text{ cm/sec}$. For simplicity, and in view of the discussion in section 1.3.6 the function



(a)



(b)

Figure 2.2 Velocity-electric field curves
(a) GaAs (b) functions assumed
in the present analysis

used in the present analysis is given in Figure 2-2(b) (curve 1). This is a piecewise linear approximation, which neglects the negative differential mobility region. This approximation is appropriate for "pentode like" operation devices (section 1.3.6), namely, for $a < W_{th}$ (eq. 1-57) (for these thin devices Gunn domains do not form). For thicker devices Gunn domains form near the drain electrode. An approach to handle this situation is outlined later in this report. The function represented by curve 2 in Figure 2-2(b) is a smooth approximation with a continuous derivative at $2E_c$. This curve is used in chapter 3.

The various curves in Fig. 2-2 represent the relationship between the magnitudes of velocity and electric field. It is further assumed that \bar{V} and \bar{E} are colinear, thus yielding the relationship between the cartesian components:

$$v_x(E) = \frac{E_x}{E} v(E) \quad (2-10)$$

$$v_y(E) = \frac{E_y}{E} v(E) \quad (2-11)$$

$$\text{where,} \quad E = \sqrt{E_x^2 + E_y^2} \quad (2-12)$$

Yamaguchi and Koderia [1] solved the above equations numerically as mentioned in Section 1.3.6. From these results they suggested a parametric function for the charge carrier concentration $n(x,y)$. Using this function in Equation 2-1 yields an analytical solution to the potential function $\psi(x,y)$. The details are given in the next section.

2.3 THE APPROXIMATE CHARGE CARRIER DENSITY FUNCTION

As described in chapter 1 much work has been done in the last few years on the numerical simulation of GaAs FET characteristics. Examination of charge carrier density plots generated by many workers (i.e. Yamaguchi and Kodera [1], Kennedy and O'Brien [5], Barnes [14]) shows that the Shockley assumption of subdividing the device into two regions (channel and depletion) is invalid for the high frequency devices considered here. In fact, there is an obvious transition region in which the charge carrier density changes gradually from N_D in the channel to zero in the depletion region. Based on the above, Yamaguchi and Kodera suggested subdividing the device into the three regions shown in Figure 2-3:

1. channel ($n=N_D$): $0 \leq y < d_1(x)$
2. transition : $d_1(x) \leq y < d_1(x) + d$
3. depletion ($n=0$): $d_1(x) + d \leq y \leq a$

The charge carrier density is approximated in the transition region by the function:

$$n(x,y) = N_D [1 - \alpha(x-\gamma)] \frac{1 + \cos \frac{\pi}{d}(y - d_1(x))}{2} \quad (2-13)$$

where,

$$d = 6 \lambda_D \text{ (see eq. 1-46), } \alpha \begin{cases} = 0 & \text{for } x < \gamma \\ \neq 0 & \text{for } x > \gamma \end{cases}$$

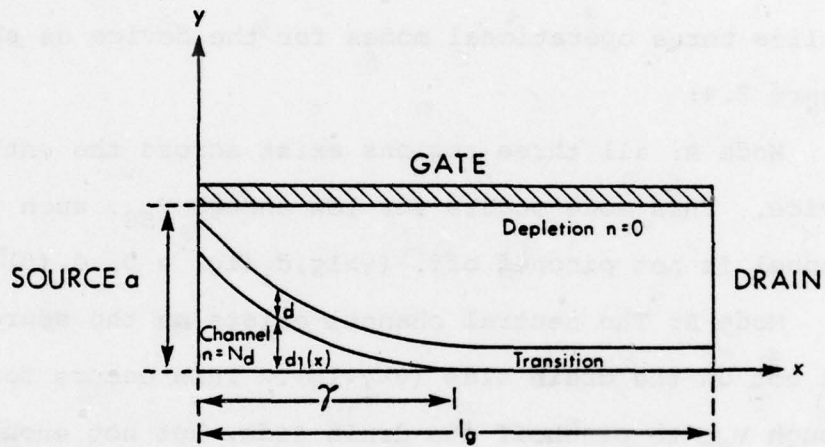


Figure 2.3 Subdivision of FET active region

The function $d_1(x)$ and the parameters α, γ are determined by using the boundary conditions, as described in the next section. Now by substituting the assumed $n(x,y)$ in Equation 2-1 one obtains a relatively simple differential equation, which can be solved analytically. There are, of course, three different equations, one for each of the regions.

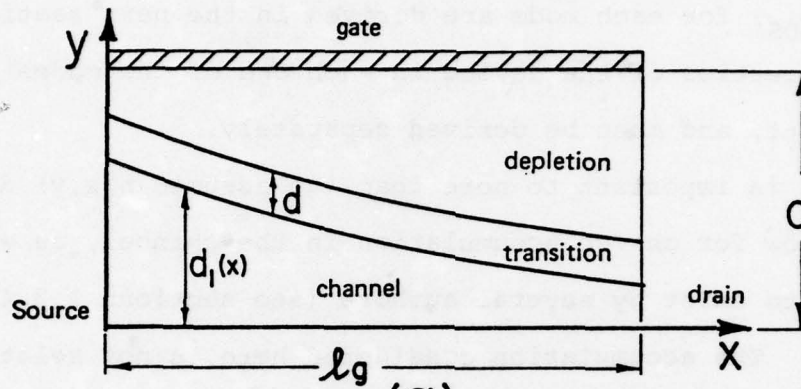
It is important to note that the suggested $n(x,y)$ implies three operational modes for the device as shown in Figure 2.4:

Mode A: all three regions exist across the entire device. This mode occurs for low enough V_{SG} , such that the channel is not pinched off. ($\gamma > l_g, d_1(l_g) > 0, d_1(0) > 0$)

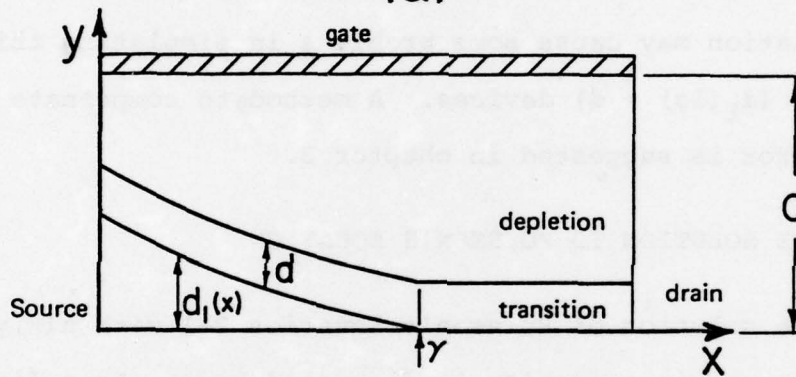
Mode B: The neutral channel exists on the source side, but not on the drain side ($0 < \gamma < l_g$). This occurs for large enough V_{SG} to pinch off the drain side, but not enough to pinch off the source side. ($d_1(l_g) = 0, d_1(0) > 0$)

Mode C: The neutral channel does not exist anywhere across the device ($\gamma < 0$). This occurs for large enough V_{SG} to pinch off the channel. The device is not cutoff, since there is some charge transport via the transition region ($d_1(0) = d_1(l_g) = 0$).

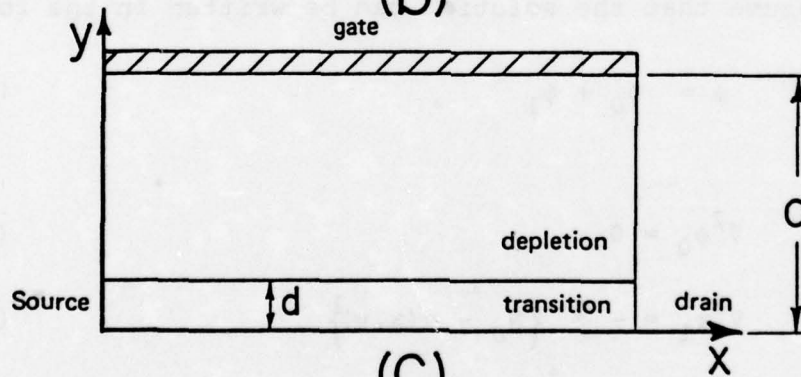
There is, of course, also operational mode D in which the device is cutoff. The exact driving conditions



(a)



(b)



(c)

Figure 2.4 Operational modes of FET

(V_{SG} , V_{DS}) for each mode are derived in the next sections. The properties of the device in each one of the modes are different, and must be derived separately.

It is important to note that the assumed $n(x,y)$ does not allow for charge accumulation in the channel, as was proven to exist by several authors (see sections 1.3.4, 1.3.6). The accumulation considered here is not related to Gunn domains but to current continuity. Neglecting this accumulation may cause some problems in simulating thick channel ($d_1(lg) > d$) devices. A method to compensate for this error is suggested in chapter 3.

2.4 THE SOLUTION TO POISSON'S EQUATION

The solution of Poisson's Equation 2-1 with $n(x,y)$ from the previous section is discussed here. As a first step assume that the solution can be written in the form

$$\psi = \psi_0 + \psi_1 \quad (2-14)$$

where,

$$\nabla^2 \psi_0 = 0 \quad (2-15)$$

$$\nabla^2 \psi_1 = -\frac{q}{\epsilon} \{N_D - n(x,y)\} \quad (2-16)$$

the boundary conditions:

$$\psi_0(0,0) = \psi_1(0,0) = 0 \quad (2-17)$$

$$\psi_0(x,a) = 0 \quad (2-18)$$

$$\psi_1(x,a) = -(\phi_B + V_{SG}) \quad (2-19)$$

$$\frac{\partial \psi_0(x,0)}{\partial y} = \frac{\partial \psi_1(x,0)}{\partial y} = 0 \quad (2-20)$$

Also define V_1, V_0 as:

$$V_1 = \psi_1(lg,0) \quad V_0 = \psi_0(lg,0) \quad (2-21)$$

$$V_1 + V_0 = V_{DS} \quad (2-22)$$

ψ_0 is the solution to Laplace's equation and can be written generally as:

$$\psi_0 = \sum_m \psi_{0m} \sinh\left(\frac{m\pi}{2a} x\right) \cos\left(\frac{m\pi}{2a} y\right) \quad (2-23)$$

For simplicity in this analysis, only the first term of the series is used (see [1]):

$$\psi_0 = \frac{V_0}{\sinh\left(\frac{\pi lg}{2a}\right)} \sinh\left(\frac{\pi x}{2a}\right) \cos\left(\frac{\pi y}{2a}\right) \quad (2-24)$$

Since the solution to ψ_1 depends on $n(x,y)$, it has to be treated separately for each region:

1. neutral channel ($n=N_D$, excess charge = zero) ($0 < y < d_1(x)$). Due to charge neutrality and boundary condition (2-20) ψ_1 is a linear function of x :

$$\psi_1 = f(x) = C_1 x + C_2 \quad (2-24)$$

To simplify the following derivations, an assumption is made that $d_1(x)$ decreases gradually in the x direction, namely:

$$\frac{\partial^2 d_1(x)}{\partial x^2} < < 1 \quad (2-25)$$

Also along the interface between the channel and transition region ($y=d_1(x)$) ψ_1 and $\frac{\partial \psi_1}{\partial y}$ should be continuous.

2. Transition region ($d_1(x) < y < d_1(x) + d$)

Using (2-25) and the continuity requirements the solution:

$$\begin{aligned} \psi_1 = & -\frac{qN_D}{4\epsilon}(y-d_1(x))^2 + \frac{qN_D}{2\epsilon}\left(\frac{d}{\pi}\right)^2 \left\{ 1 - \cos \frac{\pi(y-d_1(x))}{d} \right\} + \\ & + \frac{qN_D}{\epsilon} \alpha(x-y) \left\{ \frac{1}{2}\left(\frac{d}{\pi}\right)^2 \cos \frac{\pi(y-d_1(x))}{d} - \frac{(y-d_1(x))^2}{4} \right\} + f(x) \end{aligned} \quad (2-26)$$

3. Depletion region ($d_1(x) + d < y < a$)

Similarly, the solution for this region is:

$$\begin{aligned} \psi_1 = & -\frac{qN_D}{2\epsilon} \{y - (d_1(x) + d)\}^2 - \frac{qN_D}{2\epsilon} d \{y - (d_1(x) + d)\} \{1 + \alpha(x - \gamma)\} + \\ & + \frac{qN_D}{\epsilon} d^2 \left(\frac{1}{\pi^2} - \frac{1}{4}\right) - \frac{qN_D}{\epsilon} \frac{d^2}{4} \left(1 + \frac{2}{\pi^2}\right) \alpha(x - \gamma) + f(x) \end{aligned} \quad (2-27)$$

The validity of 2-26, 2-27 can be easily verified by substitution in 2-1 and using 2-25. Condition 2-25 turns out to cause some problems in the solution. This condition is generally satisfied everywhere except at $x = \gamma$

(see Figure 2-4(b)). At this point $\frac{\partial d_1(x)}{\partial x}$ jumps from a non-zero value to zero; thus the second derivative is infinite there. It was found that this discontinuity causes discontinuities in the capacitance, g_m, g_d and other functions which depend on derivatives of $d_1(x)$ as the device switches from mode B to mode C. Thus, some compensation is required to avoid this discontinuity. It is described in chapter 3.

Equations 2-24, 2-26, 2-27 include the following parameters: C_1, C_2, α, γ and the function $d_1(x)$. These must be determined before the solution is considered complete. Note also that in mode A and the region $0 < x < \gamma$ of mode B, the third term of 2-26 and the fourth term of 2-27 are zero since $\alpha=0$. Also, in the region

$\gamma < x < l_g$ of mode B and mode C, $d_1(x) = 0$,

The quantities C_1 and C_2 are determined by using the boundary condition at $x=0$ and l_g (2-17, 2-21), which yield:

$$C_1 = \frac{V_1}{l_g} \quad (2-28)$$

$$C_2 = 0 \quad (2-29)$$

Now use condition 2-19 in eq. 2-27 (with $\alpha=0$) and get the function $d_1(x)$:

$$d_1(x) = a - \frac{d}{2} - \sqrt{\frac{2\epsilon}{qN_d} \left\{ \frac{V_1}{l_g} x + V_{SG} + \phi_B \right\} + \left(\frac{2}{\pi^2} - \frac{1}{4} \right) d^2} \quad (2-30)$$

The pinchoff voltage, V_p , is defined as the value of V_1 which sets $d_1(l_g) = 0$. From Equation (2-30) get:

$$V_p = \frac{qN_d}{2\epsilon} \left[(a-d)^2 + d(a-d) + \left(\frac{1}{2} - \frac{2}{\pi^2} \right) d^2 \right] - (\phi_B + V_{SG}) \quad (2-31)$$

Thus, for $V_1 < V_p$ - operational mode A

for $V_1 > V_p$ - operational mode B, C or D

Also, in the region $\gamma < x < l_g$ of mode B, ψ_1 at $y=a$ is equal to $-(\phi_B + V_{SG})$, from condition (2-19). Inserting this into 2-27 and using 2-31 yields:

$$f(x) = \frac{qN_D}{\epsilon} \left(\frac{ad}{2} - \frac{d^2}{4} + \frac{d^2}{2\pi^2} \right) \alpha (x-\gamma) + V_P \quad (2-32)$$

However, $f(x)$ was already evaluated as $\frac{V_1}{1g} X$ (Equations 2-28, 2-29), so now α and γ can be evaluated by equating the two expressions.

Define:

$$\beta = \frac{qN_D}{\epsilon} \left(\frac{a}{2} - \frac{d}{4} + \frac{d}{2\pi^2} \right) d \quad (2-33)$$

Then:

$$\alpha = \frac{V_1}{\beta 1g} \quad (2-34)$$

$$\gamma = 1g \frac{V_P}{V_1} \quad (2-35)$$

Thus far, all the parameters in the solution of ψ_1 are expressed in terms of a single parameter V_1 . The solution to ψ_0 is expressed in terms of the parameter $V_0 = V_{DS} - V_1$. So, the solution to $\psi = \psi_1 + \psi_0$ is complete once V_1 is known.

The parameter V_1 is determined by using condition 2-9, namely, conduction current continuity. To apply this condition one must derive the electric field expressions at the source and drain side. Then use Equation 2-3 to derive the current density expressions. This is complicated by the nonlinearity of the v - E relationship

(velocity saturation - Figure 2-2). Then integrate the current density expressions along the source and drain electrodes and obtain the source and drain current expressions, expressed in terms of the parameter V_1 .

Now, find V_1 such as the two currents are equal.

The above process is quite lengthy, and is generally done in a numerical fashion, namely the equation $I_S = I_D$ is solved by using numerical methods such as Newton-Raphson. This is the approach employed by Yamaguchi and Koderia [1]. Thus, even though an approximate analytic solution has been achieved for the FET, the determination of the parameter is done numerically.

This situation has been rectified, and in chapter 3 a method of achieving an almost analytic solution for V_1 is presented. The method is considered almost analytic, since it has been found that the results are improved by employing one additional numerical iteration after the approximate analytic data is calculated. This new method was found to be about one order to magnitude faster than Yamaguchi and Koderia's numerical approach. A typical computation time for a given pair of (V_{SG}, V_{DS}) is about 0.1 seconds on an IBM 360. This fact makes the new model practical for circuit design, in which the model has to be called typically tens of thousands of times.

For the rest of this chapter it is assumed that the parameter V_1 has been evaluated, thus yielding a complete solution for the potential, ψ , and charge carrier concentration, n . In the next section expressions are derived for the displacement currents at the device terminals. The expressions for conduction current are derived in chapter 3, since they are closely related to the procedure of determining the parameter V_1 .

2.5 DISPLACEMENT CURRENT EXPRESSIONS

The expressions for the electric potential $\psi(x,y)$, which were derived in the previous section, can be used to derive expressions for the electric field $\bar{E} = -\nabla\psi$. The procedure is straight forward and appendix 8.1 contains a full listing of the electric field expressions at the drain, source and gate for each one of the three operational modes and in each region (channel, transition, depletion).

The above expressions can be used to calculate the displacement current at each of the electrodes for all the operational modes. The displacement current density is defined:

$$\bar{J}_D = \epsilon \frac{\partial \bar{E}}{\partial t} \quad (2-36)$$

By taking the time derivative of the expressions in appendix 8.1 $\frac{\partial \bar{E}}{\partial t}$ can be calculated. Integrating \bar{J}_D over

the proper electrode yields the displacement current via this electrode. This procedure is demonstrated here for the gate displacement current in operational mode A. The expressions for the other electrodes and operational modes are derived in a similar fashion.

The displacement current density at the gate for mode A is calculated by taking the time derivative of Equation 8.1-12:

$$j_D = \epsilon \frac{\partial E_y}{\partial t} = \epsilon \frac{\pi/2a}{\sinh(\frac{\pi l_g}{2a})} \sinh\left(\frac{\pi x}{2a}\right) \frac{\partial V_0}{\partial t} + \sqrt{\frac{qN_D}{2\epsilon(\frac{V_1}{l_g}x + V_{SG} + \phi_B)}} \left(\frac{x}{l_g} \frac{\partial V_1}{\partial t} + \frac{\partial V_{SG}}{\partial t}\right) \quad (2-37)$$

In 2-37 the expression for $d_1(x)$ (Equation 2-30) was used.

The total displacement current at the gate is calculated by integrating:

$$I_{DIS} = W \int_{x=0}^{l_g} j_D dx \quad (2-38)$$

Using also $V_0 = V_{DS} - V_1$ (W = device width) get:

$$I_{DIS} = \epsilon W \left[KGS \frac{dV_{SG}}{dt} + KDS \frac{dV_{DS}}{dt} + KG \frac{dV_1}{dt} \right] \quad (2-39)$$

where:

$$KGS = \sqrt{\frac{qN_D}{2\epsilon}} \frac{2}{V_1} \frac{1}{g} (\sqrt{V_1 + V_{SG} + \phi_B} - \sqrt{V_{SG} + \phi_B}) \quad (2-40)$$

$$KDS = [\cosh(\frac{\pi 1g}{2a}) - 1] / \sinh(\frac{\pi 1g}{2a}) \quad (2-41)$$

$$KG = \sqrt{\frac{qN_D}{2\epsilon}} \frac{2}{V_1} \frac{1}{g} \left\{ \sqrt{V_1 + V_{SG} + \phi_B} - \frac{2}{3V_1} [(V_1 + V_{SG} + \phi_B)^{3/2} - (V_{SG} + \phi_B)^{3/2}] \right\} - KDS \quad (2-42)$$

Equation 2-39 is not the final expression since it includes the time derivative of the parameter V_1 . As mentioned above, the procedure for determining V_1 is described in chapter 3. Since V_1 is an implicit function of V_{SG} and V_{DS} :

$$\frac{dV_1}{dt} = \frac{\partial V_1}{\partial V_{SG}} \frac{dV_{SG}}{dt} + \frac{\partial V_1}{\partial V_{DS}} \frac{dV_{DS}}{dt} \quad (2-43)$$

define:

$$K1 \equiv \frac{\partial V_1}{\partial V_{SG}} \quad K2 \equiv \frac{\partial V_1}{\partial V_{DS}} \quad (2-44)$$

Then, Equation 2-39 becomes:

$$I_{DIS} = \epsilon W [(KGS + KG \cdot K1) \frac{dV_{SG}}{dt} + (KDS + KG \cdot K2) \frac{dV_{DS}}{dt}] \quad (2-45)$$

The variables K_1 , K_2 are calculated by taking the time derivative of the defining equation for V_1 . This procedure is described in chapter 3. Equation 2-45 is the final expression for the gate displacement current in operational mode A. It expresses the above current as a function of the terminal voltages (V_{SG} , V_{DS}) and their time derivatives.

The displacement current expressions for the other electrodes and other operational modes are listed in appendix 8.2.

3. THE NOVEL FET MODEL FOR THE ACTIVE REGION

3.1 INTRODUCTION

This chapter presents the method used in the new FET model to determine the parameter V_1 , which appears in the solution for ψ and n , and therefore, in all relevant expressions. As mentioned in chapter 2, V_1 is calculated by equating the source and drain conduction current. Therefore, the exact expressions for these currents as a function of V_1 are derived. Due to the complexity of these equations, it is impossible to solve for V_1 analytically. Next, some approximations are made, which allow simplification of the conduction current expressions, and eventually enable an approximate analytic solution for V_1 to be obtained.

An improvement to the approximate solution is achieved by adding an additional numerical corrective iteration. For typical microwave devices one corrective iteration is sufficient. As seen in section 2.5 expressions are needed for the derivatives of V_1 with respect to V_{SG} and V_{DS} . These expressions are derived using the exact conduction current expressions, because this yields more accurate results (derivatives are much more sensitive to errors than the function itself). Also, since V_1 is already known it is reasonable to use the exact expressions.

Also, considered in this chapter is a modification in the equations caused by the use of a smooth velocity-electric field curve, and another modification to allow for a small charge accumulation at the drain side of the channel.

3.2 CASE CLASSIFICATION INDUCED BY VELOCITY-ELECTRIC FIELD CURVE

The assumed charge carrier velocity dependence on the electric field is as shown in Figure 2-2(b) (curve 1). This is a piecewise linear approximation, which considers a constant mobility, μ_0 , for $E < E_c$ and a constant velocity for $E > E_c$. Since the conduction current expressions are different for constant mobility and constant velocity, there are three different cases to be considered:

case 1: $E < E_c$ no velocity saturation at either source and drain.

case 2: $E < E_c$ at the source, but $E > E_c$ at the drain.

case 3: $E > E_c$ at both source and drain.

The case $E > E_c$ at the source, but $E < E_c$ at the drain is identical to case 2, except for the interchange of drain and source. Therefore, it is not considered a separate case. It is important to note, that the "test-point" for the source electric field is at $(x=0, y=0)$, and for the drain electric field is at $(x=l, y=0)$. As seen in the equations in appendix 8.1 the electric field generally increases with y , such that even if at the "test point" $E < E_c$, the

electric field may exceed E_c for a large enough y . This is considered further in the next section.

Since, there are three different operational modes for the device (as described in chapter 2), and for each mode there are three different cases (as described in the present section), there is a total of 9 different cases in each of which the FET is characterized by a different set of equations.

3.3 EXACT CONDUCTION CURRENT EXPRESSIONS

To demonstrate the calculation of the conduction current, outlined below is the derivation for operational mode C-case 2, namely, the case of velocity saturation at the drain, but not at the source. From Figure 2-4(c) it is obvious that the contribution to the conduction current in mode C comes only from the transition region.

3.3.1 Source Conduction Current

The electric field on the source side (transition region) is given by Equations 8.1-19 and 8.1-20; which are duplicated here for convenience:

$$E_x = - \left[\frac{V_1}{l_g} (1 + K_{Y1} \{2\cos\theta - \theta^2\}) + K_{Y2} V_o \cos(d_1\theta) \right] \quad (3-1)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} [\theta - \sin\theta + K_c (\theta + \sin\theta)] \quad (3-2)$$

where,

$$\theta = \frac{\pi y}{d} \quad (3-3)$$

$$K_{y1} = \frac{qN_D}{4\epsilon\beta} \left(\frac{d}{\pi}\right)^2 \quad (3-4)$$

$$K_{y2} = \frac{\pi/2a}{\sinh(\frac{\pi l g}{2a})} \quad (3-5)$$

$$K_c = -V_p/\beta \quad (3-6)$$

$$d_1 = d/2a \quad (3-7)$$

In case 2, which is considered here $E(o) < E_c$, namely,

$$E(o) = |E_x(o)| = \frac{V_1}{lg}(1+2K_{y1}) + K_{y2} \cdot V_o < E_c \quad (3-8)$$

However, as y increases E_y increases, and for large enough y , $E(o,y)$ may be larger than E_c . The critical $\theta = \tilde{\theta}$ at which $E(o,y) = E_c$ is defined by the equation:

$$E_x^2(\tilde{\theta}) + E_y^2(\tilde{\theta}) = E_c^2 \quad (3-9)$$

Equation 3-9 can be solved for θ numerically (Newton-Raphson) if V_1 is known. When employing a numerical solution for V_1 in an iterative fashion a value for V_1 is assumed to start with and this value is corrected each iteration. Thus in equation (3-8) the current value of

V_1 is used to solve for $\tilde{\theta}$. For the analytic solution $\tilde{\theta}$ is estimated, as described later in this chapter.

In the range $0 < \theta < \tilde{\theta}$ the velocity is not saturated and the contribution to the drift conduction current is calculated as follows. The drift current density is given by (Equation 2-3).

$$j_x = -qnV_x = -qn\mu_o E_x \quad (3-10)$$

The electron density n at the transition region is given by Equation 2-13. Using the appropriate expressions for α , γ and $d_1(x)=0$ the expression for n at the source is:

$$n_{\text{source}} = N_D [1-K_C] \frac{1+\cos\theta}{2} \quad (3-11)$$

Thus, the contribution to the drift current is

$$I_L = W \int_0^{\frac{\tilde{\theta}d}{\pi}} j_x dy = \frac{Wd}{\pi} \int_0^{\tilde{\theta}} j_x d\theta \quad (3-12)$$

Inserting 3-1 and 3-11 in 3-12 yield the solution:

$$\begin{aligned} I_L = & CD1CP (1-K_C) (\tilde{\theta} + \sin\tilde{\theta}) V_1 + \\ & + CDOC (1-K_C) [\sin(d_1\tilde{\theta}) + d_3 \sin(d_2\tilde{\theta}) + d_5 \sin(d_4\tilde{\theta})] \cdot V_o \end{aligned} \quad (3-13)$$

where,

$$CD1CP = \frac{qN_d W d \mu_o}{2\pi l g} \quad (3-14)$$

$$CDOC = \frac{qN_D \mu_o W}{2 \sinh(\frac{\pi l g}{2a})} \quad (3-15)$$

$$d_2 = 1 + d_1 \quad (3-16)$$

$$d_3 = d_1 / (2d_2) \quad (3-17)$$

$$d_4 = 1 - d_1 \quad (3-18)$$

$$d_5 = d_1 / (2d_4) \quad (3-19)$$

In the region $\tilde{\theta} < \theta < \pi$ the electron velocity is saturated; thus (see Equation 2-10):

$$j_x = -qnV_x = -qnv_s \frac{E_x}{\sqrt{E_x^2 + E_y^2}} \quad (3-20)$$

Inserting n from 3-11 into 3-20 and integrating over the range $\tilde{\theta} < \theta < \pi$ yields the drift current contribution from the upper region:

$$I_U = CD2CP \cdot (1 - K_c) \cdot \int_{\tilde{\theta}}^{\pi} \frac{(1 + \cos\theta) d\theta}{\sqrt{1 + (E_y/E_x)^2}} \quad (3-21)$$

where

$$CD2CP = \frac{qN_D v_s W d}{2\pi} \quad (3-22)$$

In Equation 3-21 the expressions for E_x , E_y are taken from equations 3-1 and 3-2. The integration in equation 3-21 can be performed numerically when V_1 is

known. In the analytic solution this integral is approximated by an analytic function, as described later in this chapter. Figure 3-1 illustrates the above mentioned partitioning of the transition region at the source side.

The diffusion current density is given by (see Equation 2-3)

$$j_{DIF} = qD\nabla n \quad (3-23)$$

$$J_{DIF_x} = qD(\nabla n)_x \quad (3-24)$$

The diffusion coefficient, D , is in general a function of the electric field. To simplify calculations, and since the electric field at the source for the case considered is quite low (less than 3.2 KV/cm), an average low-field constant value is assumed; $D_L = 250\text{cm}^2/\text{sec}$. The expression for $(\nabla n)_x = \frac{\partial n}{\partial x}$ is derived from Equation 2-13 with the appropriate expressions for α , γ and $d_1(x) = 0$:

$$\left. \frac{\partial n}{\partial x} \right|_{\text{source}} = - \frac{N_D V_1}{2\beta l g} (1 + \cos\theta) \quad (3-25)$$

Using 3-25 in 3-24 and integrating yields:

$$I_{DIF} = W \int_0^d j_{DIF_x} = \frac{Wd}{\pi} \int_0^\pi j_{DIF_x} d\theta = C_{DIFF} \cdot V_1 \quad (3-26)$$

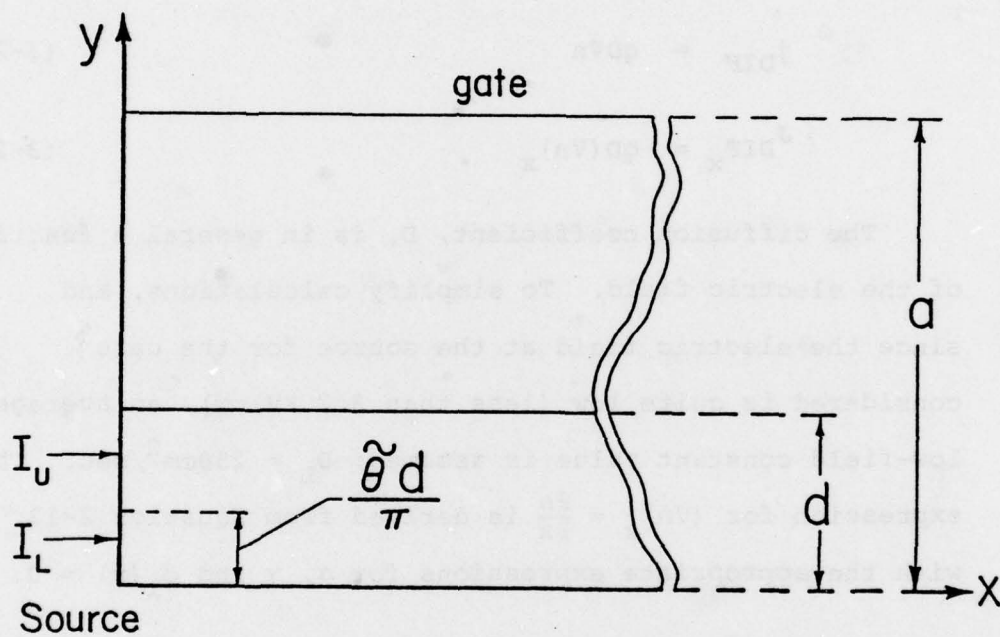


Figure 3.1 Partitioning of the transition region at the source side

where,

$$CDIFF = \frac{qD_L N_D W d}{2\beta l g} \quad (3-27)$$

Thus, the total source conduction current is given by the sum of equations 3-13, 3-21, 3-26

$$I_{con_s} = I_L + I_U + I_{DIF} \quad (3-28)$$

3.3.2 Drain Conduction Current

The electric field on the drain side (transition region) is given by Equations 8.1-14 and 8.1-15, which are duplicated here for convenience:

$$E_x = -\left[\frac{V_1}{lg}(1+Ky_1\{2\cos\theta-\theta^2\}) + K_h \cdot V_O \cos(d_1\theta)\right] \quad (3-29)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} \left[\theta - \sin\theta + \frac{V_1 - V_P}{\beta} (\theta + \sin\theta)\right] + \frac{\pi V_O}{2a} \sin(d_1\theta) \quad (3-30)$$

where θ , Ky_1 are defined by Equations 3-3 and 3-4 and

$$K_h = \frac{\pi}{2a} \coth\left(\frac{\pi lg}{2a}\right) \quad (3-31)$$

In the case considered here ($E_{drain} > E_c$) the electron velocity is saturated, thus the drift current density is:

$$j_x = -qnV_x = -qnV_s \frac{E_x}{\sqrt{E_x^2 + E_y^2}} \quad (3-32)$$

The expression for the electron density is derived from Equation 2-13 with the proper α , γ and $d_1(x)=0$:

$$n_{\text{drain}} = N_D \left[1 - \frac{V_1 - V_P}{\beta} \right] \frac{1 + \cos \theta}{2} \quad (3-33)$$

Inserting 3-33 into 3-32 and integrating over the drain ($y=0$ to d) gives:

$$I_{\text{DRIFT}} = CD2CP \cdot \left(1 - \frac{V_1 - V_P}{\beta} \right) \int_0^{\pi} \frac{(1 + \cos \theta) d\theta}{\sqrt{1 + (E_y/E_x)^2}} \quad (3-34)$$

CP2CP is given by equation (3-22) and the expressions for E_x , E_y to be used in 3-34 are given in Equations 3-29, 3-30.

The diffusion current density is given by (see equation 2-3)

$$j_{\text{DIF}_x} = qD \frac{\partial n}{\partial x} \quad (3-35)$$

For simplicity, the diffusion coefficient on the drain side is assumed a constant equal to a high-field average $D_H = 50 \text{ cm}^2/\text{sec}$. The expression for $\frac{\partial n}{\partial x}$ is derived by the same method as in the source side. The result was found to be the same as for the source (3-25).

Integrating 3-35 yields the solution:

$$I_{\text{DIF}} = CDIFFH \cdot V_1 \quad (3-36)$$

where,

$$CDIFFH = \frac{qD_H W N_D d}{2\beta l g} \quad (3-37)$$

So, the total drain conduction current is given by the sum of Equations 3-34, 3-36:

$$I_{\text{con}_d} = I_{\text{DRIFT}} + I_{\text{DIF}} \quad (3-38)$$

3.3.3 Numerical Solution For V_1

To solve for the parameter V_1 define the function

$$f(V_1) = I_{\text{con}_s} - I_{\text{con}_d} \quad (3-39)$$

The right value for V_1 sets $f(V_1)=0$, namely, it equalizes the source and drain conduction currents. From the expression derived above it is obvious that $f(V_1)$ is a quite complex function of V_1 , so that an analytic solution to $f(V_1)=0$ is unlikely to be found. However, a numerical solution is straight forward using the Newton-Raphson approach: choose an initial guess for V_1 and proceed iteratively using the iteration equation:

$$V_{1,i+1} = V_{1,i} - \left. \frac{f(V_1)}{df/dV_1} \right|_i \quad (3-40)$$

This approach was adopted by Yamaguchi and Koderia [1]. There is another approach which can be employed, especially if the initial guess is quite close to the final solution. The approach is to substitute for V_1 in the equation $f(V_1)=0$ the initial guess only in the expressions, which are complicated functions of V_1 (i.e. the integrals).

In the other expressions of the above equation keep the unknown V_1 . The equation thus derived is a simple equation for V_1 (either linear or quadratic), and is readily solved. This process can be repeated iteratively by each time substituting for V_1 in the exact equation $f(V_1)=0$ the last value computed and solving the resulting simple equation. This method is not guaranteed to converge generally. However, if it converges it can save computation time, since it does not employ derivatives. In the computer model presented in this work, the above method was employed successfully for the corrective iteration, as discussed later in this chapter.

The iteration equation in the above approach for the operational mode C-case 2, which was employed in the model, is:

$$V_{1i+1} = \frac{1}{2} \left[V_{1i} + \frac{(1-K_c) [CD2CP (DINT-SINT) - CDOC \cdot KDO \cdot V_{DS}]}{(1-K_c) [CD1CP (\tilde{\theta} + \sin \tilde{\theta}) - CDOC \cdot KDO] + CDIFF - CDIFFH + \frac{CD2CP}{\beta} DINT} \right] \quad (3-41)$$

DINT is the drain integral (Equation 3-34), SINT is the source integral (Equation 3-21). Both of them are calculated numerically using V_{1i} .

K_c , CD2CP, CDOC, CD1CP, CDIFF, CDIFFH are defined in Equations 3-6, 3-22, 3-15, 3-14, 3-27, 3-37, respectively, and

$$KDO = \sin(d_1\tilde{\theta}) + d_3\sin(d_2\tilde{\theta}) + d_5\sin(d_4\tilde{\theta}) \quad (3-42)$$

Equation 3-41 employs computation of the source and drain integrals by using the previous iteration value for V_1 . Also an averaging process is included, namely, taking the average of two consecutive iterations. This was found to improve convergence and avoid possible oscillations.

The integrations were performed numerically by partitioning the integration region into 20 parts and using the simple rule:

$$\int_0^{\tilde{\theta}} f(\theta) d\theta \approx \sum_{i=1}^{20} f(\theta_i) \Delta\theta_i \quad (3-43)$$

Twenty partitions were found to give adequate accuracy. For testing purposes 100 partitions were employed, and the result thus obtained was within 1-2% of the result obtained with 20 partitions.

3.4 ANALYTIC EXPRESSIONS FOR CONDUCTION CURRENT AND V_1

In this section some approximations are made which enable the source and drain conduction currents to be expressed as analytic functions of V_1 , and thus permit V_1 to be solved analytically. The approach is demonstrated for mode C - case 2, as in the previous section.

3.4.1 Source Conduction Current

This subsection follows the same steps as 3.3.1, except that approximations are introduced when necessary to achieve an analytic solution. First an estimate is derived for the critical angle $\tilde{\theta}$. The exact defining equation is 3-9. For $E_x=0$ 3-9 becomes $E_y=E_c$ or:

$$\theta_1 - \sin\theta_1 + K_c(\theta_1 + \sin\theta_1) = S_1$$

where:

$$S_1 = \frac{2\pi E_c \epsilon}{qN_D d} \quad (3-44)$$

Equation 3-44 is solved for θ_1 numerically by Newton-Raphson. This equation is very suitable for this method, and the convergence is very fast. For $E_x=E_y$ 3-9 becomes $E_y = E_c/\sqrt{2}$ or:

$$\theta_2 - \sin\theta_2 + K_c(\theta_2 + \sin\theta_2) = s_1/\sqrt{2} \quad (3-45)$$

This equation is solved for θ_2 as above. The estimate for the actual critical angle is:

$$\tilde{\theta} = (\theta_1 + \theta_2)/2 \quad (3-46)$$

Since Equation 3-13 for the lower region contribution is analytic in V_1 , it is kept unchanged. The contribution of the upper part is given by Equation 3-21, which is a complicated function of V_1 . Therefore it must be

estimated by an analytic expression. To achieve this goal, consider the ratio of the total drift current to the lower part contribution (Equation 3-13) with $\tilde{\theta}$ from equation (3-46). The following assumptions are made:

1. In the E_x expression (3-1) the V_0 term is negligible. For a typical device this introduces negligible error since Ky_2 is very small (division by a sinh function).

2. Consider the above ratio for $E_x = E_c$ (or $\frac{V_1}{1g} \approx E_c$, since V_0 term is neglected). In this case the ratio is a general function almost independent of device geometry. The ratio thus achieved is used as an estimate in general, and not just for $E_x = E_c$.

Under the above assumption, the ratio function becomes:

$$R = \frac{\int_0^\pi \frac{(1+\cos\theta)d\theta}{\sqrt{1+(E_y/E_x)^2}}}{\tilde{\theta} + \sin\tilde{\theta}} \quad (3-47)$$

where:

$$\left(\frac{E_y}{E_x}\right)^2 = \left[A \frac{\theta - \sin\theta + K_c(\theta + \sin\theta)}{1 + K_{y1}(2\cos\theta - \theta^2)} \right]^2 \quad (3-48)$$

$$A = 1/S_1 \quad (3-49)$$

In general R depends on the parameters K_c , A , K_{y1} . Therefore, it was calculated numerically versus the above

parameters. The results are plotted in appendix 8.3. The parameter K_{y1} is normally very small for GaAs (0.02-0.03). and the ratio function was found to be practically independent on it in the following range of the other two parameters: $0 \leq K_C \leq 1$ in the mode C (see Equation 3-11, for $K_C=0$ $n_{\max}=N_D$, for $K_C=1$ $n=0$), A depends on the doping level (for example $A=5.76$ for $N_D=10^{17} \text{ cm}^{-3}$, $A=1.8$ for $N_D=10^{16} \text{ cm}^{-3}$). Thus, in appendix 8.3 the ratio function is plotted versus K_C with N_D (or A) as a parameter.

The above functions were approximated by a fifth order polynomial. This was achieved by using curve fitting, yielding:

$$R(K_C) + RRO + RR1 \cdot K_C + RR2 \cdot K_C^2 + RR3 \cdot K_C^3 + RR4 \cdot K_C^4 + RR5 \cdot K_C^5 \quad (3-50)$$

The six coefficients RRO , $RR1$...are functions of N_D . This dependence is given in appendix 8.3. Thus, the estimate for the total source drift current is

$$I_{\text{DRIFT SOURCE}} = R(K_C) \cdot I_L \quad (3-51)$$

where I_L is given in equation 3-13.

The diffusion current is given in Equation 3-26, and since it is a simple expression, it may be kept unchanged. However, for consistency it was estimated in the actual calculation. In the course of similar approximations performed for modes A and B it was necessary to estimate

the diffusion current in order to achieve an analytic solution for V_1 . It was found that a reasonable estimate was 7% of the V_1 term of the drift current. In mode C this assumption is not necessary, but for consistency and to avoid discontinuity it was employed there too. Since in FETs the diffusion current is generally much smaller than the drift current, the above assumption is not expected to introduce any appreciable error. Also, as mentioned above, an additional corrective numerical iteration is employed using the exact current expression. Thus, finally, the estimated source conduction current is given by:

$$I_{con_s} \approx [1.07 CD1CP \cdot (1-K_c) (\tilde{\theta} + \sin \tilde{\theta}) \cdot V_1 + CDOC \cdot (1-K_c) \cdot KDO \cdot V_o] \cdot R(K_c) \quad (3-52)$$

3.4.2 Drain Conduction Current

The exact drift drain current is given by Equation 3-34. To achieve an analytic expression the integral in the above expression must be estimated subject to simplifying assumptions:

1. In the E_x expression (Equation 3-29) the V_1 term is neglected. This is a reasonable assumption in the case considered (no velocity saturation at source, and velocity saturation at drain) since V_1 is typically a small number

($\approx 0.5V$) so $V_O = V_{DS} - V_1$ is usually larger than V_1 . Also the V_O coefficient is usually much larger than the V_1 coefficient, since $\frac{\pi}{2a} \gg \frac{1}{lg}$.

2. $\coth(\frac{\pi lg}{2a}) \approx 1$. This holds for practical microwave devices.

Under the above assumptions:

$$\left(\frac{E_Y}{E_X}\right)^2 = \left[\frac{\theta - \sin\theta + l_3(\theta + \sin\theta)}{l_1 \cos(l_2\theta)} + \tan(l_2\theta) \right]^2 \quad (3-53)$$

where:

$$l_1 = \frac{\pi^2 \epsilon V_O}{q N_D d a} \coth\left(\frac{\pi lg}{2a}\right) \quad (3-54)$$

$$l_2 = \frac{d}{2a} \quad (3-55)$$

$$l_3 = \frac{V_1 - V_P}{\beta} \quad (3-56)$$

Consider the integral:

$$I = \int_0^\pi \frac{(1 + \cos\theta) d\theta}{\sqrt{1 + (E_Y/E_X)^2}} \quad (3-57)$$

The expression from 3-53 is used in 3-57. This integral is a function of the three parameters l_1, l_2, l_3 . Note that for $l_1 \rightarrow 0$, $I \rightarrow 0$. Also for $l_1 \rightarrow \infty$ $(\frac{E_Y}{E_X}) \rightarrow \tan(l_2\theta)$ and the integral can be solved analytically. The result is:

$$\begin{aligned} \mu_1(\ell_2) = I = & \frac{1}{\ell_2} \sin(\ell_2 \pi) + \frac{1}{2(1+\ell_2)} \sin[(1+\ell_2)\pi] \\ & + \frac{1}{2(1-\ell_2)} \sin[(1-\ell_2)\pi] \end{aligned} \quad (3-58)$$

The integral function is investigated in appendix 8.4. It is calculated numerically (100 partitions) in the range:

$$0 \leq \ell_1 \leq 5 \text{ (with limiting value for } \infty \text{ from 3-58)}$$

$$\ell_2 = 0.15, 0.4$$

$$0 \leq \ell_3 \leq 1$$

An attempt was made to approximate the function by an exponential, as described in appendix 8.4, and the best fit to the data was achieved by the function:

$$I \approx \mu_1 [1 - \mu_2 e^{0.3835 - 2.414 \ell_1}] \quad (3-59)$$

μ_1 is given in Equation 3-58 and:

$$\mu_2 = 1 + 4.798 \ell_3 \quad (3-60)$$

The above approximation was found to be reasonably accurate for $\ell_1 \geq 1$. As $\ell_1 \rightarrow 0$ the approximation fails. This is not a serious problem since as mentioned above, for the case consider here V_0 is large enough, so that

practically ℓ_1 is larger than 1. If a situation occurs in which $\ell_1 < 1$, the solution achieved using the following equations is inaccurate, and this may require more than one corrective iteration. In the course of using the model to analyze typical high-frequency devices the largest number of corrective iterations which had to be used was 2.

Thus, using the approximation of 3-59 in 3-34 get:

$$I_{\text{con}_d} = CD2CP \cdot \mu_1 (1 - \ell_3) [1 - (1 + 4.798\ell_3)e^{-2.414\ell_1}]^{0.3835} \quad (3-61)$$

where μ_1 is defined in 3-58 and ℓ_1, ℓ_2, ℓ_3 are defined in 3-54, 55, 56.

As done in the approximation for the source current, here too the diffusion current is estimated. Since $D_H = 0.2D_L$, the diffusion current on the drain side is only 20% of that on the source side. On the source side the diffusion current was estimated at 7% of the drift current. Thus, the diffusion current on the drain side is slightly over 1% of the drift current. So, for the purpose of the analytic approximation the diffusion current at the drain side is negligible. Therefore, the expression in Equation 3-61 is an approximation of the total drain conduction current.

3.4.3 Analytic Solution For V_1

The analytic expressions for the source and drain conduction current which were derived above can be used to get an analytic solution for the parameter V_1 .

Define the equation:

$$I_{\text{con}_s} = I_{\text{con}_d} \quad (3-62)$$

where I_{con_s} is expressed in Equation 3-52 and I_{con_d} is expressed in Equation 3-61. The I_{con_s} expression is a simple linear function of V_1 (set $V_o = V_{DS} - V_1$). However, the I_{con_d} expression contains an exponential dependence on V_1 (through ℓ_1) and a quadratic dependence on V_1 (through ℓ_3). Neglecting temporarily the exponential dependence, equation (3-62) is basically a simple quadratic equation in V_1 , whose solution is straight forward. To solve the exponential dependence problem, in Equation 3-62 substitute V_{DS} instead of V_o in the expression for ℓ_1 . This is justified, since a) V_o for the case considered here is usually larger than V_1 (as discussed in the previous section) so $V_o \approx V_{DS}$ ($V_o = V_{DS} - V_1$); and b) the drain integral (see appendix 8.4) is a slowly varying function of ℓ_1 for large ℓ_1 ($\ell_1 > 2$).

Under the above assumptions Equation 3-62 can be written in the form:

$$A V_1^2 - B V_1 + C = 0 \quad (3-63)$$

where:

$$A = \frac{4.798f}{\beta} \quad (3-64)$$

$$B = 1-f + \frac{4.798f}{\beta} (\beta + 2V_P) + \frac{D_1 - D_O}{G_D} \quad (3-65)$$

$$C = (\beta + V_P) \left(1-f + \frac{4.798f}{\beta} V_P \right) - \frac{D_O}{G_D} V_{DS} \quad (3-66)$$

$$f = e^{-2.414\ell_1} \quad (3-67)$$

$$\ell_1 = \frac{\pi^2 \epsilon V_{DS}}{q N_D d a} \coth\left(\frac{\pi l g}{2a}\right) \quad (3-68)$$

$$G_D = \frac{q N_D W v_s d \mu_1}{2\pi\beta} \quad (3-69)$$

$$D_1 = \frac{1.07 q N_D W d \mu_O}{2\pi l g} (1-K_C) R(K_C) (\tilde{\theta} + \sin \tilde{\theta}) \quad (3-70)$$

$$D_O = \frac{q N_D \mu_O W}{2 \sinh\left(\frac{\pi l g}{2a}\right)} (1-K_C) \cdot R(K_C) \cdot K D O \quad (3-71)$$

The solution to Equation 3-63 is:

$$V_1 = \frac{B - \sqrt{B^2 - 4 \cdot A \cdot C}}{2A} \quad (3-72)$$

In the computer model Equation 3-72 is used to calculate a reasonable estimate for the parameter V_1 , which is usually very close to the actual solution. However, due to the approximations involved in the process of achieving the analytic solution some error is expected. Therefore, as a second step in the model a better estimate for V_1 is computed by using the iterative approach with the exact equations, as described in section 3.3.3. This part of the model is numerical, however, due to the good analytic estimate given by 3-72 (zero-order-approximation), the numerical process is very short - typically one iteration. Thus, this new model is very fast (0.05-0.1 sec for a given pair of voltages V_{SG} , V_{DS} on IBM 360) and practical for circuit design.

Once the solution for V_1 is obtained the modeling problem of the active region is practically solved. The conduction current is computed using the exact source conduction current expression (Equation 3-28). The displacement current is calculated using the equations in appendix 8.2 with expressions for derivatives of V_1 as derived in the next section. The expressions for transit time, charging resistor, transconductance and drain conductance are derived in the following sections.

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3.5 EXPRESSIONS FOR V_1 DERIVATIVES

As discussed in section 2.5, the calculation of the displacement current involves the derivatives

$$K1 = \frac{\partial V_1}{\partial V_{SG}}, K2 = \frac{\partial V_1}{\partial V_{DS}}. \text{ These derivatives can be evaluated}$$

by using the defining equation for V_1 , namely

$$f(V_1) = I_{\text{con}_s} - I_{\text{con}_d} = 0, \text{ Equation 3-39. The } I_{\text{con}_s} \text{ expression}$$

is given in Equation 3-28, and I_{con_d} is given in

Equation 3-38. From an examination of the above expressions one concludes that the function $f(V_1)$ is in fact a function of the following variables: $V_1, V_{SG}, V_{DS}, \tilde{\theta}$. Now, take the time derivative of the equation $f(V_1) = 0$ and get:

$$ACV1 \cdot \frac{dV_1}{dt} + ACSVG \cdot \frac{dV_{SG}}{dt} + ACDS \cdot \frac{dV_{DS}}{dt} + ACTET \cdot \frac{d\tilde{\theta}}{dt} = 0 \quad (3-73)$$

where:

$$\begin{aligned} ACV1 = & (1 - K_c) [CD1CP \cdot (\tilde{\theta} + \sin \tilde{\theta}) - CDOC \cdot KDO + CD2CP \cdot \frac{\partial (SINT)}{\partial V_1}] + \\ & + CDIFF - CDIFFH + CD2CP \cdot DINT / \beta - CD2CP \cdot (1 - \frac{V_1 - V_P}{\beta}) \frac{\partial (DINT)}{\partial V_1} \end{aligned} \quad (3-74)$$

$$\begin{aligned} ACSVG = & [CD2CP (1 - K_c) \frac{\partial (SINT)}{\partial K_c} - CD2CP \cdot SINT - CDOC \cdot KDO \cdot V_O - \\ & - CD1CP (\tilde{\theta} + \sin \tilde{\theta}) V_1] / \beta + CD2CP \cdot DINT / \beta - CD2CP \cdot \\ & (1 - \frac{V_1 - V_P}{\beta}) \frac{\partial (DINT)}{\partial V_{SG}} \end{aligned} \quad (3-75)$$

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$$\begin{aligned} ACDS = & (1-K_C) [CDOC \cdot KDO + CD2CP \cdot \frac{\partial (SINT)}{\partial V_{DS}} - \\ & - CP2CP (1 - \frac{V_1 - V_P}{\beta}) \frac{\partial (DINT)}{\partial V_{DS}}] \end{aligned} \quad (3-76)$$

$$\begin{aligned} ACTET = & (1-K_C) [CD1CP (1 + \cos \tilde{\theta}) V_1 + CDOC \cdot V_O \cdot \frac{d(KDO)}{d\tilde{\theta}} + \\ & + CD2CP \frac{\partial (SINT)}{\partial \tilde{\theta}}] \end{aligned} \quad (3-77)$$

SINT is the source integral (Equation 3-21) and DINT is the drain integral (Equation 3-34). These integrals and their derivatives are calculated numerically (20 partitions). In the computer model SINT is computed in routine UPADER and DINT is computed in routine DRACUR. Some of the derivatives in the above expressions can be computed analytically:

$$\frac{\partial (SINT)}{\partial \tilde{\theta}} = - \frac{1 + \cos \tilde{\theta}}{\sqrt{1 + [E_y(\tilde{\theta}) / E_x(\tilde{\theta})]^2}} \quad (3-78)$$

The expressions for E_x , E_y to be used in 3-78 are given in 3-1, 3-2.

$$\frac{d(KDO)}{d\tilde{\theta}} = d_1 [\cos(d_1 \tilde{\theta}) + 0.5 \cdot \cos(d_2 \tilde{\theta}) + 0.5 \cdot \cos(d_4 \tilde{\theta})] \quad (3-79)$$

To get rid of the dependence on $\tilde{\theta}$ in Equation 3-73 it is necessary to derive another equation. This is achieved

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by using the defining equation for $\tilde{\theta}$ (Equation 3-9). Take the time derivative of equation 3-9 and get:

$$AIV1 \cdot \frac{dv_1}{dt} + AISG \cdot \frac{dv_{SG}}{dt} + AIDS \cdot \frac{dv_{DS}}{dt} + AITET \cdot \frac{d\tilde{\theta}}{dt} = 0 \quad (3-80)$$

where:

$$AIV1 = \left[\frac{1 + Ky_1 (2\cos\tilde{\theta} - \tilde{\theta}^2)}{lg} - Z \cdot \cos(d_1 \tilde{\theta}) \right] \cdot \left[\frac{V_1 \{1 + Ky_1 (2\cos\tilde{\theta} - \tilde{\theta}^2)\}}{lg} + Z \cdot V_0 \cdot \cos(d_1 \tilde{\theta}) \right] \quad (3-81)$$

$$AISG = \left(\frac{E_c}{S_1} \right)^2 \frac{\tilde{\theta} + \sin\tilde{\theta}}{\beta} [\tilde{\theta} - \sin\tilde{\theta} + Kc \cdot (\tilde{\theta} + \sin\tilde{\theta})] \quad (3-82)$$

$$AIDS = Z \cdot \cos(d_1 \tilde{\theta}) \left[\frac{V_1 \{1 + Ky_1 (2\cos\tilde{\theta} - \tilde{\theta}^2)\}}{lg} + Z \cdot V_0 \cdot \cos(d_1 \tilde{\theta}) \right] \quad (3-83)$$

$$AITET = \left(\frac{E_c}{S_1} \right)^2 \cdot \{1 - \cos\tilde{\theta} + Kc \cdot (1 + \cos\tilde{\theta})\} \cdot \{\tilde{\theta} - \sin\tilde{\theta} + Kc \cdot (\tilde{\theta} + \sin\tilde{\theta})\} -$$

$$- \left\{ \frac{2Ky_1 \cdot V_1}{lg} (\tilde{\theta} + \sin\tilde{\theta}) + Z \cdot d_1 \cdot V_1 \cdot \sin(d_1 \tilde{\theta}) \right\} \cdot$$

$$\cdot \left\{ \frac{V_1 \{1 + Ky_1 (2\cos\tilde{\theta} - \tilde{\theta}^2)\}}{lg} + Z \cdot V_0 \cdot \cos(d_1 \tilde{\theta}) \right\} \quad (3-84)$$

$$Z = \frac{\pi}{2a \cdot \sinh\left(\frac{\pi lg}{2a}\right)} \quad (3-85)$$

Combining Equations 3-73, 3-80 eliminates $\frac{d\tilde{\theta}}{dt}$ and thus expresses $\frac{dv_1}{dt}$ in terms of $\frac{dv_{SG}}{dt}$ and $\frac{dv_{DS}}{dt}$:

$$\frac{dv_1}{dt} = K1 \frac{dv_{SG}}{dt} + K2 \frac{dv_{DS}}{dt} \quad (3-86)$$

where:

$$K1 = \frac{A_{ISG} \cdot A_{CTET} - A_{CSG} \cdot A_{ITET}}{A_{CV1} \cdot A_{ITET} - A_{IV1} \cdot A_{CTET}} \quad (3-87)$$

$$K2 = \frac{A_{IDS} \cdot A_{CTET} - A_{CDS} \cdot A_{ITET}}{A_{CV1} \cdot A_{ITET} - A_{IV1} \cdot A_{CTET}} \quad (3-88)$$

The above two equations are the desired expressions for the derivatives $K1 = \frac{\partial v_1}{\partial v_{SG}}$, $K2 = \frac{\partial v_1}{\partial v_{DS}}$.

3.6 CALCULATION OF g_m AND g_d

For the purpose of small signal characterization of the FET (such as s-parameter calculation) it is necessary to compute the transconductance, g_m , and drain conductance, g_d :

$$g_m = - \frac{\partial (I_{con})}{\partial v_{SG}} \quad (3-89)$$

$$g_d = \frac{\partial (I_{con})}{\partial v_{DS}} \quad (3-90)$$

The computation is done directly from the definition, namely, taking the proper derivatives of the conduction current. In the computer model the drain conduction current expression is used (Equation 3-38). The derivation is straightforward and the expressions are:

$$g_m = \frac{CD2CP}{\beta} (1+K1) \cdot (DINT) - CDIFFH K1 - CD2CP \cdot \left(1 - \frac{V_1 - V_P}{\beta}\right) \cdot \left\{ \frac{\partial (DINT)}{\partial V_{SG}} + \frac{\partial (DINT)}{\partial V_1} \cdot K1 \right\} \quad (3-91)$$

$$g_d = CDIFFH \cdot K2 + CD2CP \left(1 - \frac{V_1 - V_P}{\beta}\right) \cdot \left\{ \frac{\partial (DINT)}{\partial V_{DS}} + \frac{\partial (DINT)}{\partial V_1} K2 \right\} - \frac{CD2CP}{\beta} (DINT) \cdot K2 \quad (3-92)$$

DINT is the drain integral (Equation 3-34). The integral and its derivatives are calculated numerically as described in the previous section. K1 and K2 are computed from equations 3-87, 3-88.

3.7 MISCELLANEOUS TOPICS

This section describes some of the problems encountered in the development of the new model and their solutions. Most of these problems are due to some imperfections of the analytic solution and the basic assumptions. Therefore, generally a complete solution was not possible, and only first order corrections were employed.

3.7.1 Correction of $\frac{\partial d_1(0)}{\partial V_{SG}}$

As discussed in section 2.4, the derivative of the function $d_1(x)$, which defines the boundary of the neutral channel and is given by equation (2-30), is continuous except at the point $x=\gamma$, where it jumps from some

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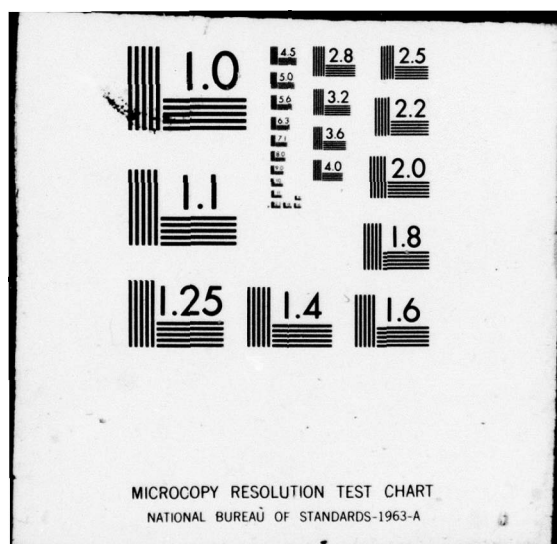
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negative value to zero (see Figure 2.4(b)). Thus the second derivative is infinite at this point, which violates assumption 2-25, and in fact, is equivalent to a surface charge located at $x=\gamma$.

The practical effect of the above is to induce a jump in the capacitances (or equivalently in the displacement current coefficients). The jump occurs as the device goes from operational mode B to operational mode C (as V_{SG} is increased). The jump is on the order of a few percent.

Since the problem arises due to a basic assumption, it is impossible to cure it completely without changing the entire solution. However, since practically the jump is not too large, it is possible to improve the situation by a first order correction as follows:

The main effect of the function $d_1(x)$ on the capacitance is via the derivative $\frac{\partial d_1(0)}{\partial V_{SG}}$. The expression for this function is derived from Equation 2-30:

$$\left. \frac{\partial d_1(0)}{\partial V_{SG}} \right|_{\text{Theory}} = - \frac{\epsilon}{qN_D (a - \frac{d}{2} - d_1(0))} \quad (3-93)$$

An attempt was made to correct the problem by adding a constant to the above expression

$$\left. \frac{d_1(0)}{V_{SG}} \right|_{\text{practice}} = - \frac{\epsilon}{qN_D (a - \frac{d}{2} - d_1(0))} - \text{CORAT1} \quad (3-94)$$

CORAT1 is a constant, which is set such as to equate the input capacitances (common source) at the boundary between modes B and C calculated from the mode B equations and mode C equations. This approach was proven successful for practical devices, and it prevents the above mentioned jump.

3.7.2 Charge Accumulation

As discussed in section 1.3.4, numerical simulations of the FET, such as Kennedy and O'Brien's [5], show that there is some charge accumulation near the drain. This happens even for silicon devices and, thus, is not due to Gunn domain formation. The accumulation presented here is based on the assumption of a neutral channel, and no allowance is made for any charge accumulation. For devices which are not too thick, the neutral channel is small and current continuity is achieved mainly by rotation of the velocity vector in the transition region. However, for thick devices the channel is thick, and most of the current is carried through it. In this case current continuity cannot be achieved only by means of velocity vector rotation, since in the channel the velocity vector is almost entirely in the X direction even for low fields. Thus, some charge accumulation is expected.

The effect of neglecting this charge accumulation in the model is to introduce a false negative slope region in the I_D - V_{DS} curve beyond the "knee" for V_{SG} around zero, as demonstrated in Figure 3.2. As V_{SG} is increased, the channel decreases, and current continuity can be achieved by rotation of the velocity vector, so the negative slope disappears.

The problem exists, of course, only for operational mode A, since in the other modes there is no neutral channel at the drain side. To solve the problem, a first order correction is proposed by assuming a small charge accumulation at the drain, which depends on the electric field as follows:

$$n = N_D \left[1 + (\text{CHAADR}) \left\{ 1 - e^{-(\text{CHADEX}) \left(\frac{E_{\text{drain}}}{E_c} - 1 \right)} \right\} \right] \quad (3-95)$$

CHAADR is a constant representing the maximum relative charge accumulation (for $E_{\text{drain}} \rightarrow \infty$), and CHADEX is an electric field constant. Equation 3-95 is used instead of N_D in the expression for the drain conduction current in the neutral channel in mode A. E_{drain} is the electric field at $(x=l, y=0)$. Thus, this correction affects the solution for V_1 , its derivatives and the expressions for g_m , g_d .

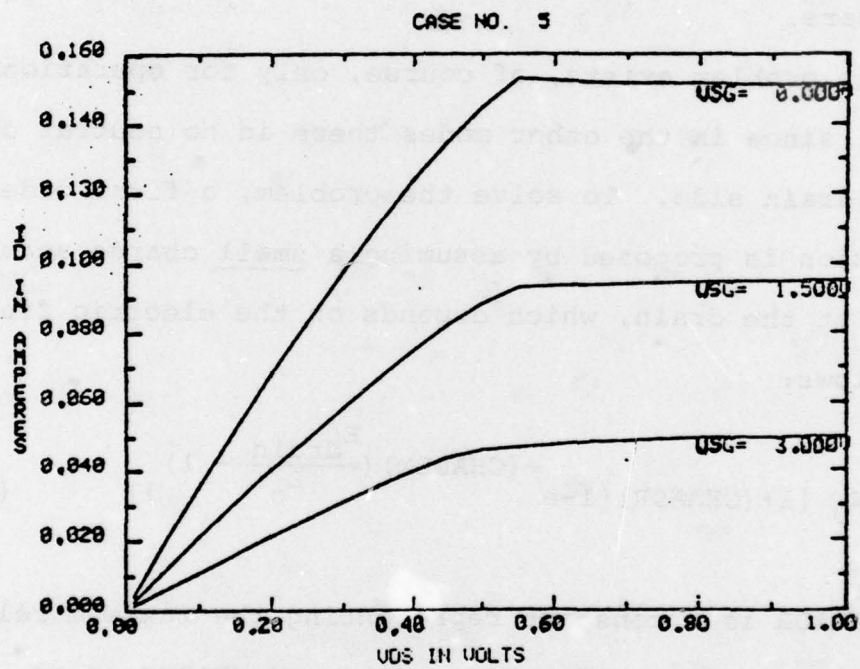


Figure 3.2 False negative slope in I_D - V_{DS} curves

The constants CHAADR, CHADEX are set so as to eliminate the negative slope region. Since the assumption of equation 3-95 is only a first order correction there is no unique way to set the constants. A convenient and effective method to do it is as follows:

- (a) Choose a value of V_{DS} 3-4 times the "knee" voltage.
- (b) Set: CHADEX = 2.
- (c) For the above V_{DS} plot g_m versus V_{SG} (zero to cutoff).
- (d) Repeat (c) with several values of CHAADR (typically 0.05-0.2) and choose that value which makes g_m almost constant in modes A, B (slightly decreasing with V_{SG}), and then sharply decreasing for mode c.
- (e) With the value of CHAADR set in (d) plot g_m versus V_{DS} ($V_{SG}=0$) for $V_{DS}=0$ to beyond the "knee".
- (f) Repeat (e) with several values of CHADEX (typically 0.5-1.0) and choose that value which makes g_m increase with V_{DS} up to the "knee" and then remains almost constant. If the plot exhibits a maximum, choose a value that minimizes that maximum.

An example of applying the above method is given in chapter 5. The correction described here was found quite effective for typical microwave devices. For very thick devices the correction is ineffective.

3.7.3 Smooth Velocity - Field Curve

As stated in chapter 2, in the entire theory presented above, the assumption was that the functional dependence of the charge-carrier velocity on the electric field is a piecewise linear function as shown in Figure 2-2(b)-curve 1. This assumption was found to cause some "cosmetic" problems in operational mode A when the channel is thick enough ($V_{SG} \approx 0$). As discussed in the previous section the rotation of the velocity vector is quite small in the neutral channel, since the electric field is almost entirely in the x-direction. Thus the problem is effectively one dimensional in the channel. Therefore, if most of the conduction current comes via the channel (only a small contribution from the transition region), the I_D - V_{DS} curve is practically a replica of the velocity-electric field curve. So, the I_D - V_{DS} curve of the FET has a "sharp corner" for $V_{SG} \approx 0$ due to the "sharp corner" in the assumed v-E curve (see Figure 3.3).

From experimentally measured I_D - V_{DS} curves of FETs it is known that the transition between the two sections at the "knee" is smooth. To get such a smooth transition for the model it is necessary to assume a smooth v-E curve. In modes B and C the transition is smooth even for the piecewise linear v-E curve since there is no neutral channel at the drain, and the effect of gradual rotation of the

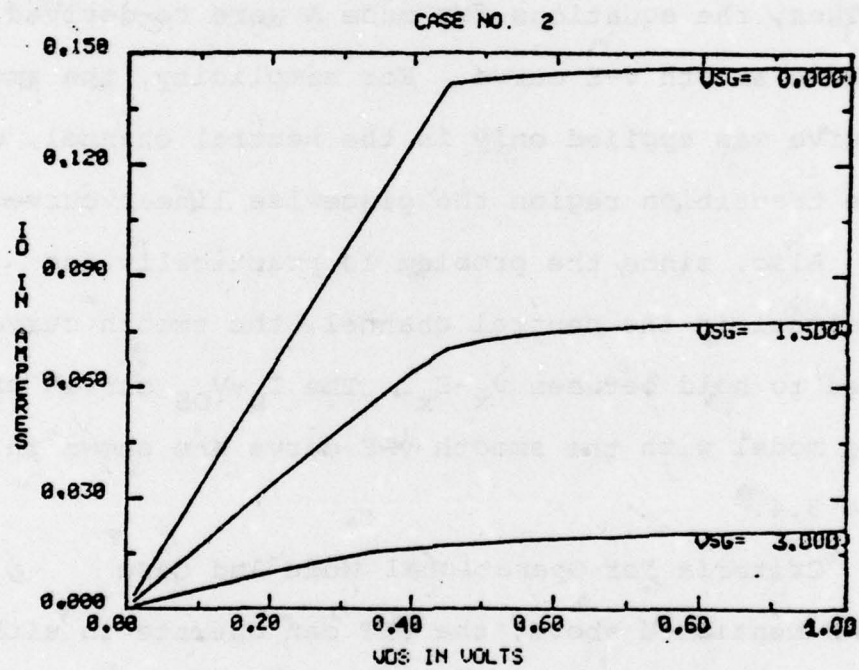


Figure 3.3 A "sharp-corner" in I_D - V_{DS} curves

velocity vector creates a smooth transition. Therefore, it is necessary to use a smooth v - E curve only for mode A. The smooth curve assumed here is the one shown in Figure 2-2(b) - curve 2. This is a parabolic function with the same initial slope as the piecewise linear curve. Physically, this means the same low-field mobility.

Thus, the equations for mode A were re-derived with the above smooth v - E curve. For simplicity, the smooth v - E curve was applied only in the neutral channel, while in the transition region the piecewise linear curve was kept. Also, since the problem is practically one dimensional in the neutral channel, the smooth curve was assumed to hold between v_x - E_x . The I_D - V_{DS} curves predicted by the model with the smooth v - E curve are shown in Figure 3.4.

3.7.4 Criteria For Operational Mode And Case

As mentioned above, the FET can operate in either one of the three operational modes (or cutoff - referred to as mode D), and in each one of these modes it can operate in either one of three cases (see section 3.2). Given a pair of voltages V_{SG} , V_{DS} the first step is to determine the operational mode and case, and then apply the proper set of equations. In this section the method to determine mode and case is outlined.

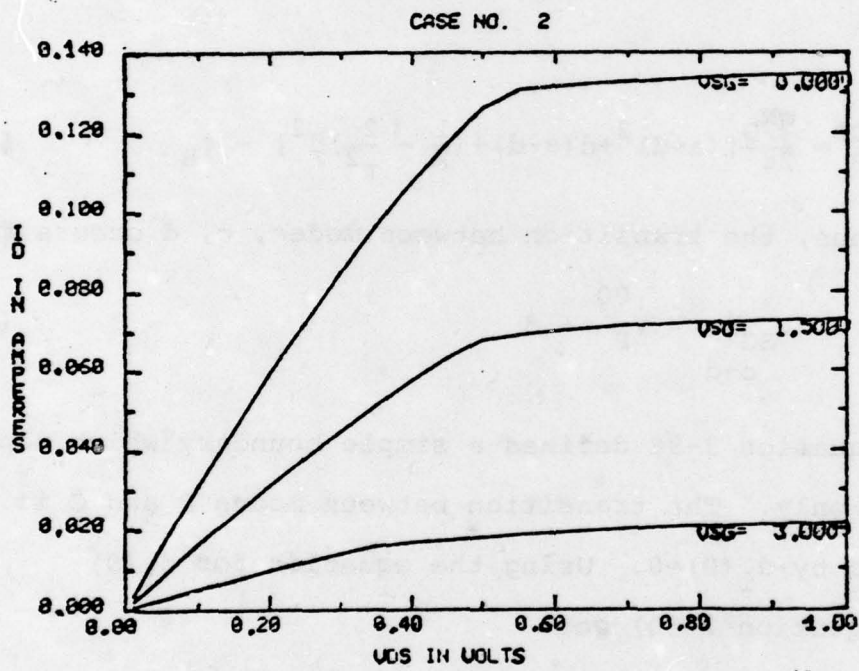


Figure 3.4 "Smooth" I_D - V_{DS} curves

The transition between mode C and mode D (cutoff) is defined by zero conduction current in both source and drain. From Equations 3-28 and 3-38 it is concluded that both currents are zero if a) $V = 0$, and b) $V_p = -\beta$. However, V_p can be written as (Equation 2-31):

$$V_p = V_p^{00} - V_{SG} \quad (3-96)$$

where:

$$V_p^{00} = \frac{qN_D}{2\epsilon} [(a-d)^2 + d(a-d) + (\frac{1}{2} - \frac{2}{\pi^2})d^2] - \phi_B \quad (3-97)$$

Thus, the transition between modes, c, d occurs for:

$$V_{SG} \Big|_{c \rightarrow d} = V_p^{00} + \beta \quad (3-98)$$

Equation 3-98 defines a simple boundary which depends on V_{SG} only. The transition between modes B and C is defined by $d_1(0)=0$. Using the equation for $d_1(0)$ (see Equation 2-30) get:

$$d_1(0) = a - \frac{d}{2} - \sqrt{\frac{2\epsilon}{qN_D} (V_{SG} + \phi_B) + (\frac{2}{\pi^2} - \frac{1}{4})d^2} = 0 \quad (3-99)$$

or after rearrangement and use of Equation 3-97:

$$V_{SG} \Big|_{B \rightarrow C} = V_p^{00} \quad (3-100)$$

The transition between modes A and B is defined by $d_1(l_g)=0$. Using Equations 2-30 and 3-97 get:

$$V_{SG} + V_1 \Big|_{A \rightarrow B} = V_P^{00} \quad (3-101)$$

Note that 3-101 is different from the other two transition conditions 3-98 and 3-100 in that it depends on both V_{SG} and V_{DS} (via V_1). Since V_1 is unknown a priori, if the pair V_{SG}, V_{DS} is such that the operational mode is found to be either A or B an estimate must be used for V_1 to decide which equations to use. This is obtained by using the approximate expression for V_1 in mode A. Applying the above yields the approximate expression

$$V_1 \approx \frac{\frac{d}{2\pi} \Delta_1 f - D_O V_{DS}}{D_1 - D_O} \quad (3-102)$$

where:

$$\Delta_1 = 3.256 - 1.063 \frac{d}{2a} \quad (3-103)$$

$$f = 1 - e^{-2.414q^{0.3835}} \quad (3-104)$$

$$q = \frac{\pi^2 \epsilon V_{DS}}{q N_D d a} \coth\left(\frac{\pi l g}{2a}\right) \quad (3-105)$$

$$D_O = \frac{\pi \mu_O [d_1(0) + DOT]}{2 a v_s \sinh\left(\frac{\pi l g}{2a}\right)} \quad (3-106)$$

$$D_1 = \frac{1.07 \mu_O [d_1(0) + D1T]}{l g v_s} \quad (3-107)$$

$$DOT = \frac{a}{\pi} \left(1.16 + 0.12 \frac{N_D (\text{cm}^{-3}) - 10^{16}}{9 \cdot 10^{16}} \right) \text{KDO} \quad (3-108)$$

$$DIT = \frac{d}{2\pi} (1.16 + 0.12 \frac{N_D (\text{cm}^{-3}) - 10^{16}}{9 \cdot 10^{16}}) (\bar{\theta} + \sin \bar{\theta}) \quad (3-109)$$

$$\bar{\theta} = \frac{1}{2} (\theta_1 + \theta_2) \quad (3-110)$$

$$\theta_1 \text{ is the solution of } \theta_1 - \sin \theta_1 = S_1 \quad (3-111)$$

$$\theta_2 \text{ is the solution of } \theta_2 - \sin \theta_2 = S_1 / \sqrt{2} \quad (3-112)$$

V_1 from equation (3-102) is used in equation (3-101) to determine the operational mode. However, since this is an approximation, when the calculations are finished the exact V_1 is inserted in (3-101) and if the initial decision is found wrong, the calculations are repeated with the correct mode equation. This can happen only for driving conditions close to the transition between modes A, B.

To sum up, the criteria for determining the operational mode are:

$$V_{SG} \geq V_P^{00} + \beta \rightarrow \text{mode D}$$

$$V_P^{00} + \beta > V_{SG} \geq V_P^{00} \rightarrow \text{mode C}$$

$$V_{SG} < V_P^{00} + \begin{cases} V_{SG} + V_1 \geq V_P^{00} \rightarrow \text{mode B} \\ V_{SG} + V_1 < V_P^{00} \rightarrow \text{mode A} \end{cases}$$

Once the operational mode is determined it is still necessary to determine the appropriate case (see section 3.2). For a typical microwave device the most common one is case 2, namely, $E_{\text{drain}} > E_c$ and $E_{\text{source}} < E_c$. Case 1 ($E_{\text{source}}, E_{\text{drain}} < E_c$) occurs only for very low V_{DS} (0.5-1v), and case 3 ($E_{\text{source}}, E_{\text{drain}} > E_c$) occurs quite rarely (typically for $\frac{lg}{a}$ ratio small).

From the equations in appendix 8.1 it is obvious that the electric field at the drain ($x=lg, y=0$) is approximately:

$$E_{\text{drain}} \approx \frac{V_1}{lg} + \frac{\pi V_0}{2a} \quad (3-113)$$

For very low V_{DS} : $E_{\text{drain}} < E_c$ (case 1). As V_{DS} increases, both V_1 and V_0 increase and eventually $E_{\text{drain}} > E_c$ (case 2). An estimate to this critical V_{DS}^c is achieved by neglecting the V_0 term ($V_1 \approx V_{\text{DS}}$).

$$V_{\text{DS}}^c = E_c \cdot lg \quad (3-114)$$

V_{DS}^c is in fact an upper limit to the critical V_{DS} , since actually V_0 is not zero and it contributes to the electric field, so that it reaches E_c for $V_{\text{DS}} < V_{\text{DS}}^c$. In view of the above, the method to determine the proper case is as follows:

- a) If $V_{DS} \leq V_{DS}^c$ choose case 1
- b) If $V_{DS} > V_{DS}^c$ choose case 2
- c) Proceed the calculation of V_1 with the chosen case equations. When V_1 is calculated compute the exact electric field at the drain.
- d) If E_{drain} is compatible with the case chosen proceed to (e). Otherwise, repeat (c) with the proper case equations.
- e) Calculate the exact source electric field.
If $E_{\text{source}} < E_c$ proceed with device properties calculations. Otherwise, repeat the calculations with case 3 equations.

4. THE COMPLETE FET COMPUTER MODEL STRUCTURE

4.1 INTRODUCTION

The modeling of the active part of the FET (under the gate metalezation), which is the most important part, was described in some detail in chapter 3. In the present chapter the complete model of the FET is presented. This model includes in addition to the active region, various parasitic elements, some of which are internal to the device, and some of which are external. The evaluation of these elements is discussed, and equations are derived for the internal elements. Also considered in this chapter is the structure of the computer model, which is constructed in modular form. The various subroutines are described and their function discussed. The input and output parameters are stated and their meaning explained. The use of the model for various applications is described.

4.2 THE MODEL

The complete model of an assembled FET chip is given in Figure 4.1. The box labeled "basic FET chip" represents the active region of the device, and is characterized as described in the previous chapters. As far as the external terminals are concerned the equations characterizing the "chip" are:

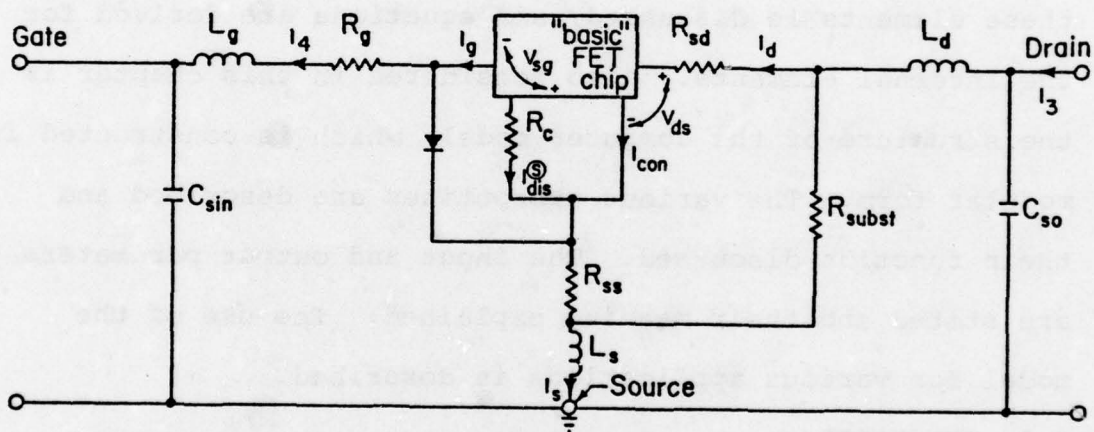


Figure 4.1 Assembled FET chip model

$$I_g = GVSG \frac{dv_{SG}}{dt} + GVDS \frac{dv_{DS}}{dt} \quad (4-1)$$

$$I_D = I_{con} + DVSG \frac{dv_{SG}}{dt} + DVDS \frac{dv_{DS}}{dt} \quad (4-2)$$

$$I_{S_{int}} = I_{con} + \underbrace{SVSG \frac{dv_{SG}}{dt} + SVDS \frac{dv_{DS}}{dt}}_{I_{dis}} \quad (4-3)$$

The internal source current is designated $I_{S_{int}}$ in equation (4-3) to distinguish it from the total source current, which includes also the diode current (to be discussed below). Of course, since $I_{S_{int}} = I_D - I_g$, the following hold:

$$SVSG = DVSG - GVSG \quad (4-4)$$

$$SVDS = DVDS - GVDS \quad (4-5)$$

The conduction current, I_{con} , and the displacement current coefficients (GVSG, GVDS, etc.) are calculated by the model as functions of V_{SG} , V_{DS} using the expressions derived in the previous chapters. For example, GVSG, which is the coefficient of $\frac{dv_{SG}}{dt}$ in the gate current equation, is found from appendix 8.2 for mode A (Equation 8.2-11):

$$GVSG = C_o (KGS + KG \cdot K1) \quad (4-6)$$

(mode A)

The other network elements in Figure 4.1 are basically parasitics, which are unwanted but also unavoidable. The external parasitics are as follows:

- C_{sin} - input stray capacitance
- C_{SO} - output stray capacitance
- L_g - gate wire bond inductance
- L_d - drain wire bond inductance
- L_s - source wire bond inductance

The wire bond inductances can usually be estimated by the physical size of the wire bond. The stray capacitances are more difficult to estimate. For a packaged device they can be characterized by measuring an empty package.

R_g is the gate metallization resistance. Usually it can be estimated quite accurately from the geometry of the gate electrode, as well as the metallization thickness and metal properties. The resistance R_g as well as the external parasitics are inputs to the model, namely, they have to be estimated and specified by the user.

The diode in Figure 4.1 represented the gate-source Schottky barrier junction. Usually the gate-source junction is reverse-biased, and the diode is not necessary. However, in some cases (such as overdriven power amplifiers or frequency multipliers, oscillators, etc.) the gate-source voltage becomes positive for a portion of the period, and there is gate conduction. To simulate this gate conduction

the diode was added to Figure 4.1. This approach (an external diode) is, of course, approximate and does not take into account any effect internal to the device due to gate conduction. The characterization of the diode is up to the user. Throughout the simulations presented in chapter 5 an ideal diode was assumed. The diode is assumed to be a short-circuit for $V_{\text{diode}} > V_{\text{on}}$ and an open circuit for $V_{\text{diode}} \leq V_{\text{on}}$. The turn-on voltage, V_{on} , is specified by the user (a typical number is 0.5 V). In all practical cases the drain to gate voltage is positive, so the drain-gate diode is excluded from Figure 4.1. In any special case, in which V_{DG} may be negative it is necessary to add this extra diode to the model (see oscillator example in chapter 5).

The two resistors R_{sd} , R_{ss} represent the bulk resistance of the epitaxial layer from the edge of the gate electrode to the drain and source electrodes, respectively (see Figure 1-4). These resistors are calculated by the simple formula:

$$R = \frac{l_{\text{eff}}}{\sigma A} \quad (4-7)$$

where, the conductivity is:

$$\sigma = qN_D\mu_0 \quad (4-8)$$

The cross-sectional area A is:

$$A = W a \quad (4-9)$$

The effective length of the resistor is estimated as the distance between the electrodes plus one-quarter of a circle of diameter a. Thus:

$$R_{ss} = \frac{lgs + \frac{\pi a}{4}}{qN_d \mu_o Wa} \quad (4-10)$$

$$R_{sd} = \frac{lgd + \frac{\pi a}{4}}{qN_D \mu_o Wa} \quad (4-11)$$

The resistances R_{ss} , R_{sd} are not computed by the FET computer model package. They must be calculated by the user in the main program using Equations 4-10, 4-11.

The resistance R_{subst} is the substrate resistance. Since the semi-insulating substrate on top of which the epitaxial layer is grown is not ideal and has some non-zero conductivity, some of the device current is carried via the substrate. In the present model, this phenomenon is not included physically. Instead, R_{subst} is added externally as in Figure 4.1. The value of R_{subst} must be specified by the user. For good substrates this effect is negligible, and a large value should be specified for R_{subst} .

R_c is an effective charging resistor through which the depletion region is charged and discharged. R_c is in series with the gate to source capacitance, thus only the displacement source current is carried by it, as shown in Figure 4.1. The calculation of R_c is described in the next section.

4.3 THE CHARGING RESISTOR

4.3.1 Introduction

As discussed in chapter 2 (section 2.2), the boundary condition 2-9, which is used to evaluate the parameter V_1 (source and drain conduction currents equal), is strictly valid for DC drive only. For AC drive, the size of the depletion region changes with time, and it is charged and discharged. The charge necessary to accomplish the above is extracted from the current between source and drain. Thus, instantaneously, the source and drain conduction currents are not equal, but there is a time delay due to the finite velocity of the charge carriers. Therefore, to compensate at least partially for the error introduced by 2-9, two parameters are introduced into the model, which are calculated for each pair of V_{SG} , V_{DS} . The parameters are: a) the time delay (transit time via the channel) and b) the effective charging resistor through which the depletion region is charged. The calculation of the time delay and

its use in the model are presented in section 4.4. The calculation of the charging resistor is described here.

4.3.2 Charging Resistance Of a Distributed Network

The FET channel is basically a distributed combination of resistors and capacitors as shown in Figure 4.2(a). Part of the charge carriers flowing from source to drain are used to charge the distributed capacitors. To investigate this "leakage" current consider the discrete distributed network in Figure 4.2(b). For simplicity, at this stage the channel is assumed to be subdivided such that all the capacitors are equal. This assumption is removed later.

For the network in Figure 4.2(b) assume that the frequency ω_0 is not too high, so that the voltage across each capacitor is approximately equal to V_M (small voltage drop across the resistors). Then the network in Figure 4.2(c) can be considered equivalent to the network in Figure 4.2(b). The effective charging resistor, R_C , is computed as follows:

Subject to the assumption above (ω_0 low enough), the current in each capacitor is $I_0 = \omega C_0 V_M$. Then, the current in R_N is I_0 , in R_{N-1} is $2I_0$...in R_1 is NI_0 . So, the total power dissipated in the network is:

$$P = I_0^2 (R_N + 4R_{N-1} + 9R_{N-2} + \dots + N^2 R_1) \quad (4-12)$$

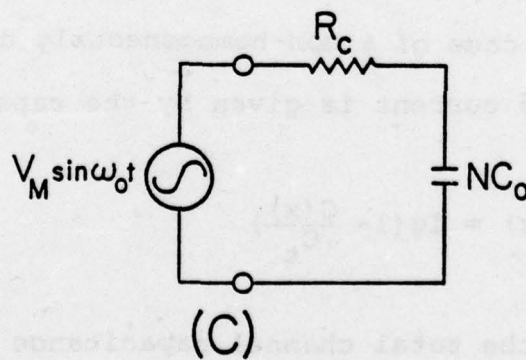
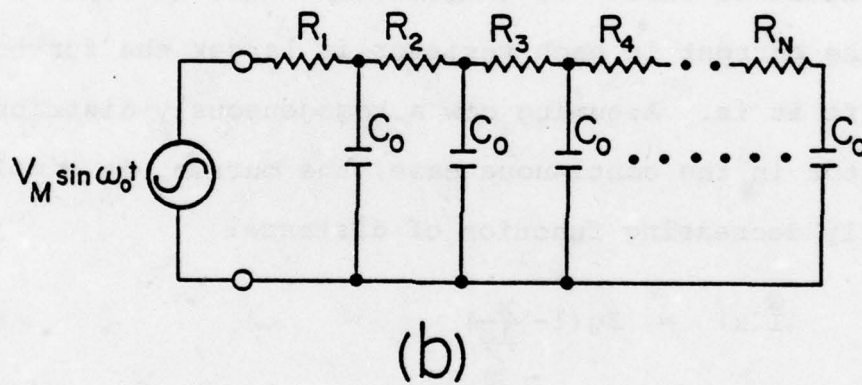
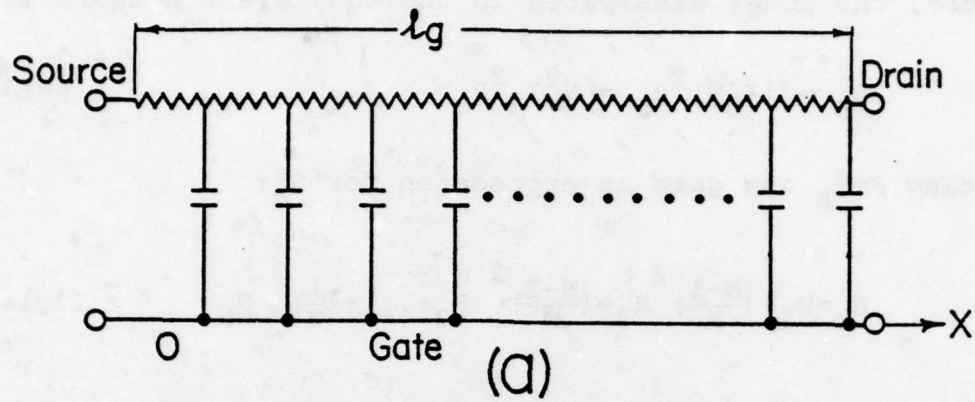


Figure 4.2 (a) FET channel as a distributed network (b) discrete distributed network considered in text (c) equivalent network

However, the power dissipated in the equivalent network is

$$P_E = (I_O N)^2 R_C = N^2 I_O^2 R_C \quad (4-13)$$

Equating $P=P_E$ one gets an expression for R_C :

$$R_C = R_1 + \left(\frac{N-1}{N}\right)^2 R_2 + \left(\frac{N-2}{N}\right)^2 R_3 + \dots + \left(\frac{1}{N}\right)^2 R_N \quad (4-14)$$

A similar result can be achieved now by returning to the continuous case. In the discrete case it was shown that the current in each resistor is larger the further to the left it is. Assuming now a homogeneously distributed capacitor in the continuous case, the current is simply a linearly decreasing function of distance:

$$I(x) = I_g \left(1 - \frac{x}{l_g}\right) \quad (4-15)$$

where I_g is the generator current.

For the case of a non-homogeneously distributed capacitor the current is given by the capacitance ratio:

$$I(x) = I_g \left(1 - \frac{C(x)}{C_t}\right) \quad (4-16)$$

where C_t is the total channel capacitance and $C(x)$ is the portion of channel capacitance between 0 to x ($x=0$ at the source).

Using the same approach as in the discrete case, the power dissipated in the network is calculated. The power dissipation in the small portion of the channel between x and $x+dx$ is:

$$dP = I_g^2 \left(1 - \frac{C(x)}{C_t}\right)^2 R(x) dx \quad (4-17)$$

$R(x)$ is the channel resistance per unit length.

Thus,

$$P = I_g^2 \int_0^{lg} \left(1 - \frac{C(x)}{C_t}\right)^2 R(x) dx \quad (4-18)$$

In the equivalent network (Figure 4.2(c)):

$$P_E = I_g^2 R_C \quad (4-19)$$

Equating $P=P_E$ get:

$$R_C = \int_0^{lg} \left(1 - \frac{C(x)}{C_t}\right)^2 R(x) dx \quad (4-20)$$

Equation (4-20) gives the general expression for the charging resistor of the channel. To actually evaluate the resistance the proper expressions for $C(x)$, C_t , $R(x)$ must be used in 4-20. The above expressions are different for each operational mode, therefore, the charging resistor expression is different for each mode.

For the purpose of calculating $C(x)$, C_t and $R(x)$ for each mode, the FET is divided into channel and depletion regions. The transition region is not considered here. Actually, half of it is "attached" to the channel and the other half to the depletion region, as demonstrated in Figure 4.3. Thus the effective channel height is $d_1(x) + \frac{d}{2}$, and the rest of the device is assumed to be depletion region.

4.3.3 Mode A

The capacitance of an element of the depletion region between x and $x+dx$ is

$$dC = \epsilon W \frac{dx}{a - d_1(x) - d/2} \quad (4-21)$$

thus,

$$C(x) = \epsilon W \int_0^x \frac{dx}{a - d_1(x) - d/2} \quad (4-22)$$

$$\text{and so } C_t = C(lg) \quad (4-23)$$

Using Equation 2-30 for $d_1(x)$, the integral in (4-22) is solved, the function $C(x)$ determined and the ratio is found:

$$1 - \frac{C(x)}{C_t} = \frac{\sqrt{V_1 + V_{SG} + CD_{10}} - \sqrt{\frac{V_1}{lg}x + V_{SG} + CD_{10}}}{\sqrt{V_1 + V_{SG} + CD_{10}} - \sqrt{V_{SG} + CD_{10}}} \quad (4-24)$$

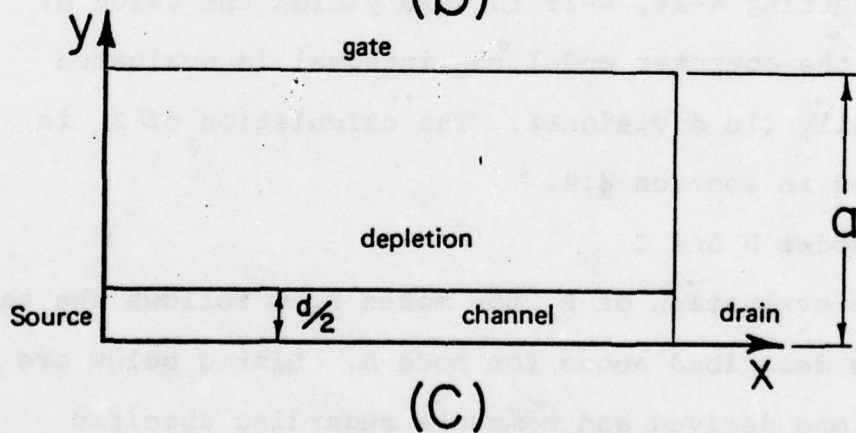
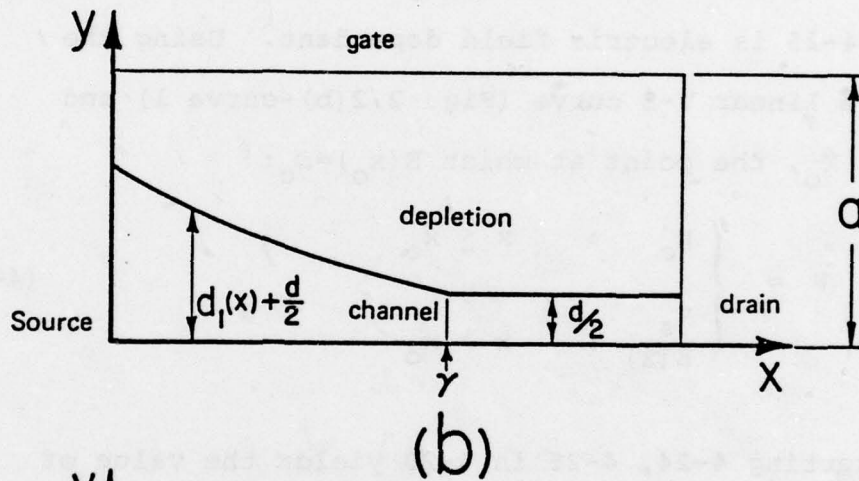
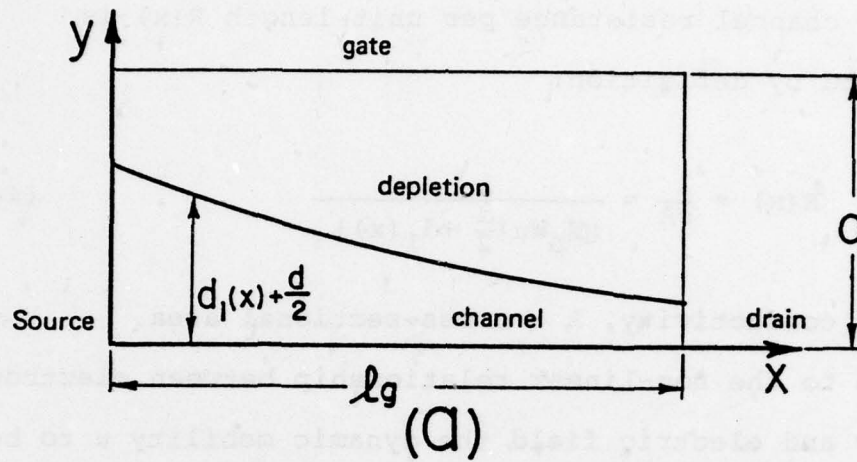


Figure 4.3 FET subdivision for charging resistor calculation (a) mode A (b) mode B (c) mode C

The channel resistance per unit length $R(x)$ is calculated by definition:

$$R(x) = \frac{1}{\sigma A} = \frac{1}{qN_D W \mu \left[\frac{d}{2} + d_1(x) \right]} \quad (4-25)$$

σ - conductivity, A - cross-sectional area.

Due to the non-linear relationship between electron velocity and electric field, the dynamic mobility μ to be used in 4-25 is electric field dependent. Using the piecewise linear V-E curve (Fig. 2.2(b)-curve 1) and defining x_0 , the point at which $E(x_0) = E_c$:

$$\mu = \begin{cases} \mu_0 & : x \leq x_0 \\ \frac{v_s}{E(x)} & : x > x_0 \end{cases} \quad (4-26)$$

Inserting 4-24, 4-25 in 4-20 yields the value of R_c . In the computer model the integral is evaluated numerically (10 divisions). The calculation of x_0 is described in section 4.4.

4.3.4 Modes B And C

The evaluation of R_c for modes B, C follows the same steps as described above for mode A. Listed below are the expressions derived and comments regarding specific problems.

In mode B the R_c expression involves two integrals, one from 0 to γ and one from γ to lg (see Figure 4.3(b)). For the first integral:

$$\frac{C(x)}{C_t} = \frac{\sqrt{\frac{2qN_D}{\epsilon}} \frac{lg}{V_1} \sqrt{\frac{V_1}{lg} x + V_{SG} + CD10} - \sqrt{V_{SG} + CD10}}{\frac{lg-\gamma}{a-\frac{d}{2}} + \sqrt{\frac{2qN_D}{\epsilon}} \frac{lg}{V_1} (\sqrt{V_P^{00} + CD10} - \sqrt{V_{SG} + CD10})} \quad (4-27)$$

The $R(x)$ expression is the same as in mode A.

For the second integral:

$$1 - \frac{C(x)}{C_t} = \frac{\frac{lg-x}{a-\frac{d}{2}}}{\frac{lg-\gamma}{a-\frac{d}{2}} + \sqrt{\frac{2qN_D}{\epsilon}} \frac{lg}{V_1} (\sqrt{V_P^{00} + CD10} - \sqrt{V_{SG} + CD10})} \quad (4-28)$$

$$R(x) = \frac{2}{qnW\mu d} \quad (4-29)$$

$$n = N_D \left[1 - \frac{V_1}{\beta lg} \left(x - lg \frac{V_P}{V_1} \right) \right] \quad (4-30)$$

μ is computed from 4-26.

In mode C:

$$\frac{C(x)}{C_t} = \frac{x}{lg} \quad (4-31)$$

and $R(x)$ is the same as in 4-29 with n from 4-30.

The problem in mode C is that the channel is partially depleted. It gets more and more depleted as V_{SG} increases up to cutoff, at which point the channel disappears. Thus, a criterion has to be established for a boundary between the channel and the depletion region. Since the drain is always more depleted than the source, it is possible to find a point $X_c < l_g$ at which the charge carrier density is so small that it can be practically considered as fully depleted. Thus, for the purpose of the charging resistor calculation the channel length is X_c rather than l_g . X_c is defined conveniently as the point at which $n(x) = 0.1 N_D$. Using Equation 4-30 this yields:

$$X_c = \frac{l_g}{V_1} (0.9\beta + V_p) \quad (4-32)$$

Thus, for $X_c > l_g$ the integral for R_c calculation is evaluated from 0 to l_g . However, for $X_c < l_g$ the upper limit for the integral is X_c . This shortening effect is incorporated in mode B as well since in mode B there is also partial depletion in the range $\gamma < X < l_g$.

4.4 TIME DELAY

Due to the finite velocity of the charge carriers in the channel, an electron entering the channel at the source side travels for a time period τ before it reaches the drain. This time period is the time delay or transit

time, and is a basic limitation of the device. Of course, the shorter the gate, the smaller is τ . For a typical microwave device, τ is on the order of 10 psec.

To calculate τ it is first necessary to calculate the point X_0 at which $E(X_0) = E_c$ along the X axis. From the analytic solution expressions of chapter 2, the electric field along the x-axis is given by

$$E_x(x,0) = \frac{V_1}{lg} + \frac{\pi V_0}{2a} \frac{\cosh(\frac{\pi x}{2a})}{\sinh(\frac{\pi lg}{2a})} \quad (4-33)$$

Set $E_x(X_0,0) = E_c$ and get an expression for X_0 :

$$X_0 = \frac{2a}{\pi} \operatorname{arc} \cosh \left[\frac{(E_c - \frac{V_1}{lg}) 2a \cdot \sinh(\frac{\pi lg}{2a})}{\pi V_0} \right] \quad (4-34)$$

Recall that:

$$\operatorname{arc} \cosh (X) = \ln[X + (X^2 - 1)^{1/2}] \quad (4-35)$$

So, the channel is subdivided into two regions:

- 1) $X_0 > X \geq 0$: $v_x = \mu_0 E_x$ constant mobility
- 2) $X \geq X_0$: $v_x = v_s$ constant velocity

The transit time for region 2 is simply

$$\tau_2 = \frac{lg - X_0}{v_s} \quad (4-36)$$

In region 1:

$$v_x = \frac{dx}{dt} = \mu_o E_x \quad (4-37)$$

$$\frac{dx}{\mu_o E_x} = dt \quad (4-38)$$

$$\int_0^{x_o} \frac{dx}{\mu_o E_x} = \int_0^{\tau_1} dt = \tau_1 \quad (4-39)$$

Equation 4-39 is used to calculate τ_1 by inserting in it E_x from equation 4-33. The resulting integral can be evaluated analytically by using integral tables. The solution is:

$$\tau_1 = \begin{cases} \frac{2a}{\pi \mu_o} \left[\frac{\pi}{2} - \arcsin \frac{B+A \cosh(\frac{\pi x_o}{2a})}{A+B \cosh(\frac{\pi x_o}{2a})} \right] \frac{1}{\sqrt{B^2-A^2}} & \text{for } B^2 > A^2 \\ \frac{2a}{\pi \mu_o} \ln \left[\frac{A+B+\sqrt{A^2-B^2} \tanh(\frac{\pi x_o}{4a})}{A+B-\sqrt{A^2-B^2} \tanh(\frac{\pi x_o}{4a})} \right] \frac{1}{\sqrt{A^2-B^2}} & \text{for } A^2 > B^2 \\ \frac{2a \lg}{\pi \mu_o V_1} \tanh(\frac{\pi x_o}{4a}) & \text{for } A=B \end{cases} \quad (4-40)$$

where:

$$A = \frac{V_1}{I_g} \quad (4-41)$$

$$B = \frac{(\pi V_O / 2a)}{\sinh(\frac{\pi l g}{2a})} \quad (4-42)$$

The total transit time is:

$$\tau = \tau_1 + \tau_2 \quad (4-43)$$

In modes B and C the shortening effect of the channel (section 4.3.4) is taken into account and the transit time is calculated from $x=0$ to X_c rather than to lg .

As obvious from the above, the time delay τ is a function of the driving voltages V_{SG} , V_{DS} . However, from the actual calculations it was found that τ is nearly constant over most of the dynamic range. To incorporate the time delay in the device equations 4-1 to 4-3, note that the main effect of this phenomenon is to delay the electrons entering at the source end. Thus in equation 4-2 the conduction current term has to be delayed by τ .

So, the instantaneous device equations are:

$$I_g(t) = GV_{SG}(t) \frac{dv_{SG}}{dt} + GV_{DS}(t) \frac{dv_{DS}}{dt} \quad (4-44)$$

$$I_D(t) = I_{con}(t-\tau) + DV_{SG}(t) \frac{dv_{SG}}{dt} + DV_{DS}(t) \frac{dv_{DS}}{dt} \quad (4-45)$$

$$I_{s \text{ int}}(t) = I_D(t) - I_g(t) \quad (4-46)$$

When τ is incorporated in the equations as above, equations 4-4, 4-5 are invalid, and the source current must be calculated by equation 4-46.

4.5 COMPUTER PACKAGE STRUCTURE

The new FET model presented in this report is practically implemented in the form of a computer subroutine package. The user has to write his own main program, which is to reflect the particular network to be analyzed or synthesized. In this section, the structure of the package is presented as well as the "communication" between the package and the user's main program. The package is written in FORTRAN IV.

The following statements must appear in the calling program:

```
COMMON/INDAT/ND,MU0,A,LG,PHB,W,EC,ER,VS
COMMON/FETCUR/ICON,GVSG,GVDS,DVSG,DVDS,SVSG,SVDS,CINCS,
*COCS,CINCG,COCG,CINCD,COCD,GM,GDD,TAU,RCHARG,RCHEFF
COMMON/NOIT/KKVSA,KKVSB,KKVSC,INVSAT,KNNVSA,KNNVSB,
*KNNVSC,KKNLDA,KKNLDB,KKNLDC
COMMON/CHARAC/CHAADR,CHADEx
REAL ND,MU0,LG,ICON
```

The common INDAT contains the parameters describing the device geometry and metallurgical properties. These

parameters must be specified by the user before any of the package subroutines are called. All physical quantities should be specified in MKS units, and so are the output variables. The meanings of the symbols are:

N_D - doping level, $\mu_0 = \mu_o$ - low field mobility (does not have to be specified by the user - it is calculated as

$\mu_o = \frac{V_s}{E_c}$), A - device thickness, LG - gate length, $PHB = \phi_B$ - built-in potential, W - device width, EC - critical electric field for velocity saturation, $ER = \epsilon_r$ - relative dielectric constant (≈ 12.5 for GaAs), VS - saturated velocity.

The common FETCUR contains the analysis results as follows: $ICON$ - conduction current, $GVSG$ to $SVDS$ - displacement current coefficients (equations 4-1 to 4-3), $CINCS = GVSG$ - input capacitance (common source), $COCS = COCG = DVDS$ - output capacitance (common source and gate), $CINCG = SVDS - SVSG$ - input capacitance (common gate), $CINCD = CINCS$ - input capacitance (common drain), $COCD = CINCG$ - output capacitance (common drain), GM - transconductance, GDD - drain conductance, TAU - time delay, $RCHARG$ - charging resistor, $RCHEFF = RCHARG + TAU / (2\pi \cdot CINCS)$ - effective resistance, which simulate both the charging and the time delay effects.

Upon exit from the package the above parameters are defined, and may be employed by the user in the network equations. The common NOIT contains variables defining the number of numerical iterations to be performed for each mode and case (section 3.2) as follows:

KKVSA - mode A case 3, KKVSB - mode B case 3, KKVSC - mode C case 3, KNNVSA - mode A case 1, KNNVSB - mode B case 1, KNNVSC - mode C case 1, KKNLDA - mode A case 2, KKNLDB - mode B case 2, KKNLDC - mode C case 2. The above 9 parameters must be specified by the user before calling the package subroutines. This can be done conveniently by subroutine SETITR to be described below. The variable INVSAT contains a code number, which specifies the mode and case of the last analysis performed. Thus, INVSAT is an output parameter. The value of INVSAT returned for each mode and case is listed in table 4.1. For mode D (cutoff) INVSAT=4.

The two parameters in common CHARAC are related to the charge accumulation correction (section 3.7.2) as specified in equation 3-95. These parameters must be specified before calling the package subroutines.

In addition to the above commons, the package employs several more commons which are used internally. The user is prohibited from using commons bearing those names. The names are: ACFCHC, SOURC, DRCOM, DRAIN, TRSTIM, CALCO2, UPCOM, CALCON, SMWDEC.

Table 4.1 Value of INVSAT for each mode and case

mode case	A	B	C
1	10	20	30
2	100	200	300
3	1	2	3

The FET package is composed of 14 subroutines, out of which only three are called by the user. The subroutines called by the user are:

SETITR - this subroutine sets the number of iterations to be employed in the computations for each mode and case, namely, it sets the parameters in the common NOIT. The calling sequence is:

CALL SETITR(JJ)

JJ is a vector of length 9, which has to be specified before calling SETITR. The first 3 locations of JJ correspond to case 1: mode A,B,C, the next three correspond to case 2: mode A,B,C, and the last three correspond to case 3: mode A,B,C.

FIRST - this subroutine calculates all the necessary constants used in the analysis. It has no parameters and the calling sequence is simply:

CALL FIRST

The subroutines SETITR and FIRST must be called in the main program (in this order) before the actual analysis

starts (However, before calling these two subroutines the parameters in the commons INDAT, NOIT and CHARAC must be defined). These two subroutines are used only once before the analysis starts, and are not called again, unless any of the device parameters are changed or the user wishes to change the number of iterations.

The actual analysis is performed by calling the subroutine MAYN:

```
CALL MAYN(VSG,VDS,V1)
```

VSG and VDS are input parameters and the analysis is performed for this pair of values. The analysis can be performed as many times as necessary by calling MAYN repeatedly with different values of V_{SG} , V_{DS} . V1 is an output parameter and contains upon exit the solution for V_1 corresponding to the current pair of values for V_{SG} , V_{DS} .

The subroutine MAYN a) determines the operational mode, b) calls the appropriate subroutines corresponding to the operational mode chosen and perform the analysis, and c) computes the time delay. The process described above is illustrated by the flow chart in Figure 4.4.

The other subroutines in the package are not called by the user, but from other subroutines. The main subroutines, in which most of the analysis is done are:

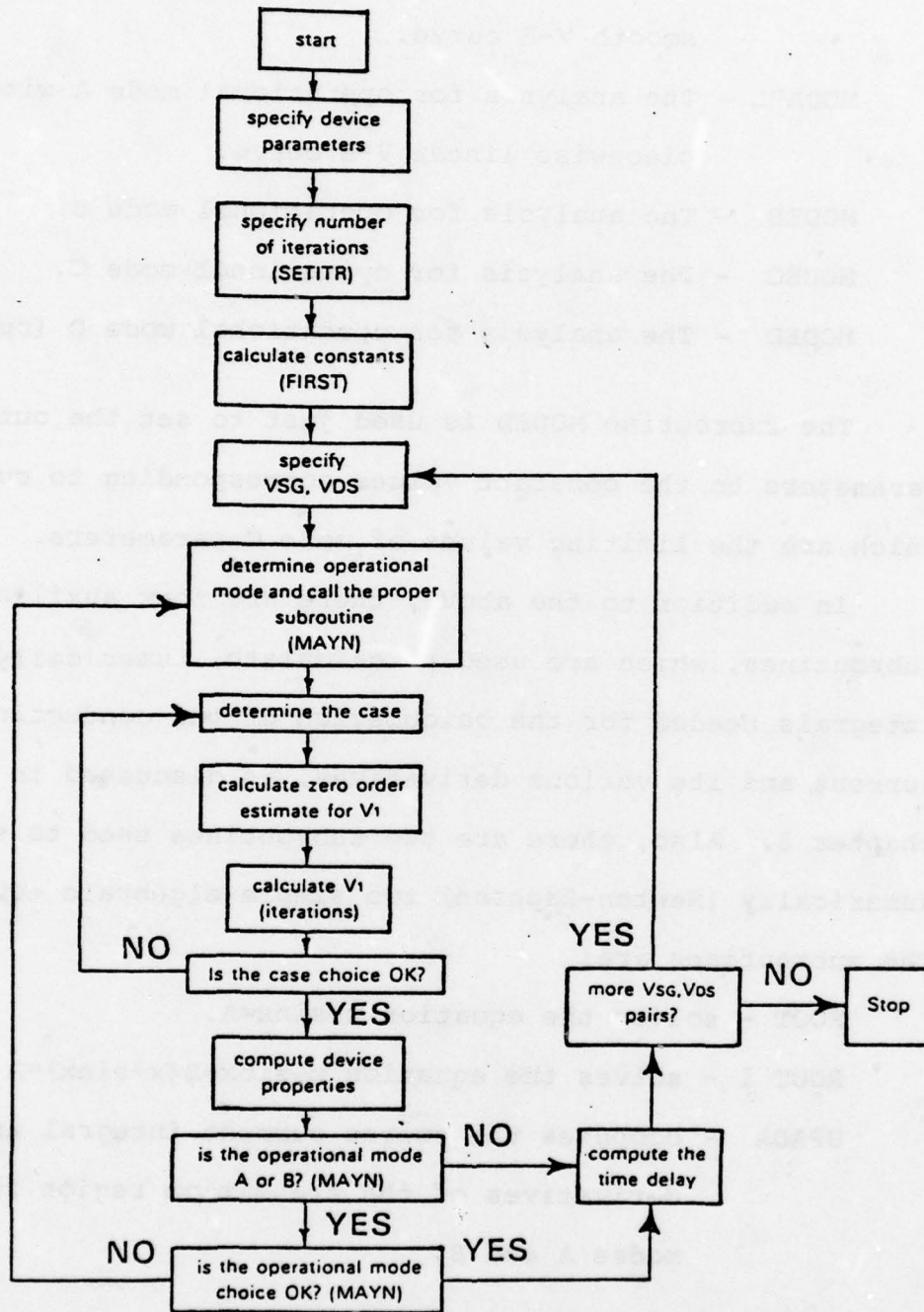


Figure 4.4 Flow chart diagram for the FET computer model

- MODASC - The analysis for operational mode A with smooth V-E curve.
- MODAPL - The analysis for operational mode A with piecewise linear V-E curve.
- MODEB - The analysis for operational mode B.
- MODEC - The analysis for operational mode C.
- MODED - The analysis for operational mode D (cutoff).

The subroutine MODED is used just to set the output parameters to the constant values corresponding to cutoff, which are the limiting values of mode C parameters.

In addition to the above, there are four auxiliary subroutines, which are used to calculate, numerically, integrals needed for the calculation of the conduction current and its various derivatives, as discussed in chapter 3. Also, there are two subroutines used to solve numerically (Newton-Raphson) two simple algebraic equations. The subroutines are:

- ROOT - solves the equation $x - \sin x = A$.
- ROOT 1 - solves the equation $x - \sin x + B(x + \sin x) = A$
- UPADA - computes the source current integral and its derivatives of the transition region for modes A and B.

UPADER - same as UPADA except for mode C.

DRCURA - computes the drain current integral and its derivatives of the transition region and channel for mode A.

DRACUR - same as DRCURA for modes B and C.

The new FET computer model is valid only for $V_{DS} \geq 0$. If a negative value for V_{DS} is used when calling MAYN the program stops with a message "VDS NEGATIVE", and the value of V_{DS} is printed. This is not a basic limitation of the model, since $V_{DS} < 0$ simply means exchange of source and drain. Thus, whenever $V_{DS} < 0$, the user can exchange the roles of drain and source, such that the new V_{DS} is positive and then use the model (see oscillator example in chapter 5).

There is no upper limit in the range of V_{SG} (it can extend to ∞). However, for $V_{SG} < 0$, the gate-source junction becomes forward biased and gate conduction occurs. V_{SG} cannot become more negative than the turn-on voltage of the (clamping) diode. This effect is taken care of automatically by the ideal diode used in the model (Figure 4-1). Since the diode is taken external to the active region, the computer model is set such that for $V_{SG} < -\phi_B$, V_{SG} is set equal to ϕ_B and the device properties calculated.

5. SIMULATION RESULTS

5.1 INTRODUCTION

In this chapter the usefulness of the model is demonstrated with several simulations. The results are presented in the form of graphs generated by the graphics package of the PDP-11/45 mini computer. The graphs were plotted on a Tektronix terminal and permanent records made with a hardcopy unit. The results presented here contain the following:

- a) DC analysis - I-V curves;
- b) small signal analysis - g_m , g_d , capacitances, S-parameters;
- and c) large signal analysis - oscillator build up and properties.

The effect of the number of iterations used is shown by performing analysis of the same device with varying number of iterations. The procedure for setting the charge correction coefficients is demonstrated on a practical device.

All the computations presented in this chapter apply for a typical microwave device, the parameters of which are presented in Table 5.1. The first 12 parameters correspond to the geometrical and material properties. The last 6 parameters correspond to the external parasitics, as well as the characteristic impedance used in the S-parameter

Table 5.1 Typical microwave FET parameters
used in the computations

CASE 2 DEVICE PARAMETERS:

- 1) GATE-SOURCE SEPERATION (LGS): 1.70 MICRONS
- 2) GATE LENGTH (LG): 1.70 MICRONS
- 3) GATE-DRAIN SEPERATION (LGD): 1.70 MICRONS
- 4) GATE WIDTH (W): 600.00 MICRONS
- 5) DOPING LEVEL (ND): $7.50E+16$ CM-3
- 6) CRITICAL ELECTRIC FIELD (EC): 3.20 KV/CM
- 7) SATURATED ELECTRON VELOCITY (VS): $1.36E+07$ CM/SEC
- 8) RELATIVE DIELECTRIC CONSTANT (ER): 12.50
- 9) BUILT-IN POTENTIAL (PHB): 0.700 VOLTS
- 10) GATE METALLIZATION RESISTANCE (RG): 2.000 OHMS
- 11) SUBSTRATE LEAKAGE RESISTANCE (RSUBST): $2.00E+05$ OHMS
- 12) EPITAXIAL LAYER THICKNESS (A): 0.3000 MICRONS

CASE 2 PACKAGE/CIRCUIT PARAMETERS:

- 1) CHARACTERISTIC IMPEDANCE (ZO): 50.0 OHMS
- 2) SOURCE INDUCTANCE (SIND): $1.00E-01$ NANOHENRIES
- 3) GATE INDUCTANCE (GIND): $5.00E-01$ NANOHENRIES
- 4) DRAIN INDUCTANCE (DIND): $2.70E-01$ NANOHENRIES
- 5) PARASITIC INPUT CAPACITANCE (SCAPIN): $1.50E-01$ PICOFARAD
- 6) PARASITIC OUTPUT CAPACITANCE (SCAPO): $1.50E-01$ PICOFARAD

calculations. These parameters correspond to the network components in Figure 4.1.

5.2 NUMBER OF ITERATIONS

As described in chapter 3, the computer model first solves for the parameter V_1 analytically, and then employs numerical iterations to improve the accuracy. Of course, since the numerical iterations are time consuming it is desirable to minimize the number of iterations which yield reasonable results. To determine this minimum it is necessary to generate I-V curves for the device with several number of iterations. The I-V curves change as the number of iterations is changed. When a reasonable convergence has been achieved the change in the curves becomes negligible as the number of iterations increases. The smallest number for which convergence is obtained is chosen as the useful number of iterations. The number of iterations for each operational mode is requested by the program.

The above procedure is demonstrated for the device considered in this chapter for operational mode A. Figure 5.1(a) presents the I-V curve in mode A ($V_{SG}=0$) without any corrective iterations. The inaccuracy in the analytic solution causes the "jump" in the curve at the point where the set of equations used is switched from case 1 to case 2. Figure 5.1(b) presents the I-V curve for the same case with one corrective iteration. This curve is smooth and does not exhibit any discontinuities.

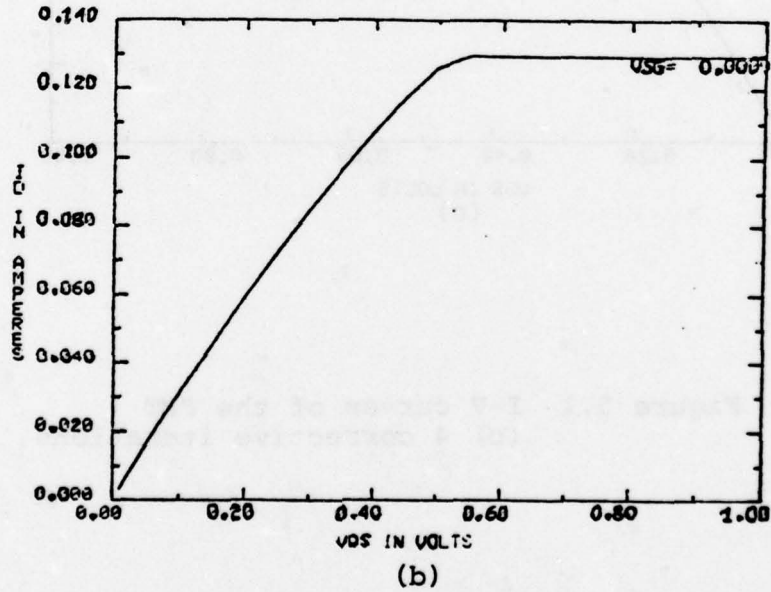
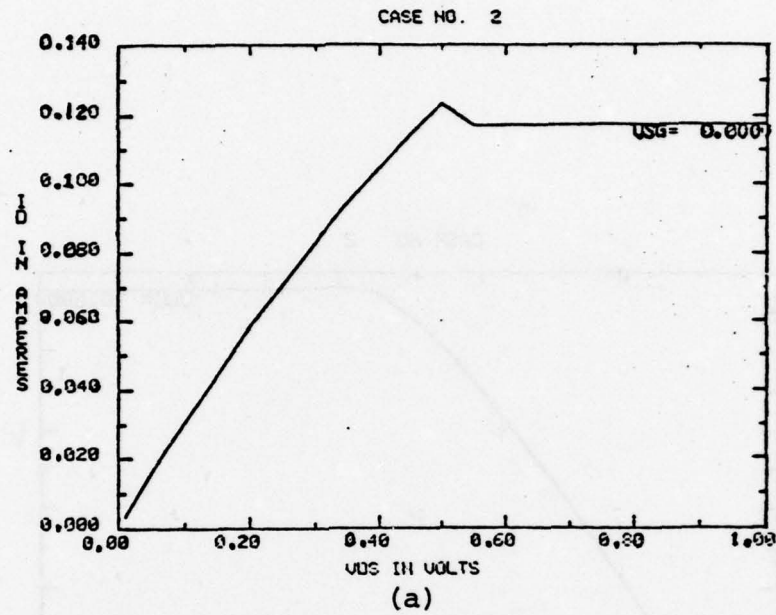


Figure 5.1 I-V curves of the FET (a) no corrective iterations (b) one corrective iteration

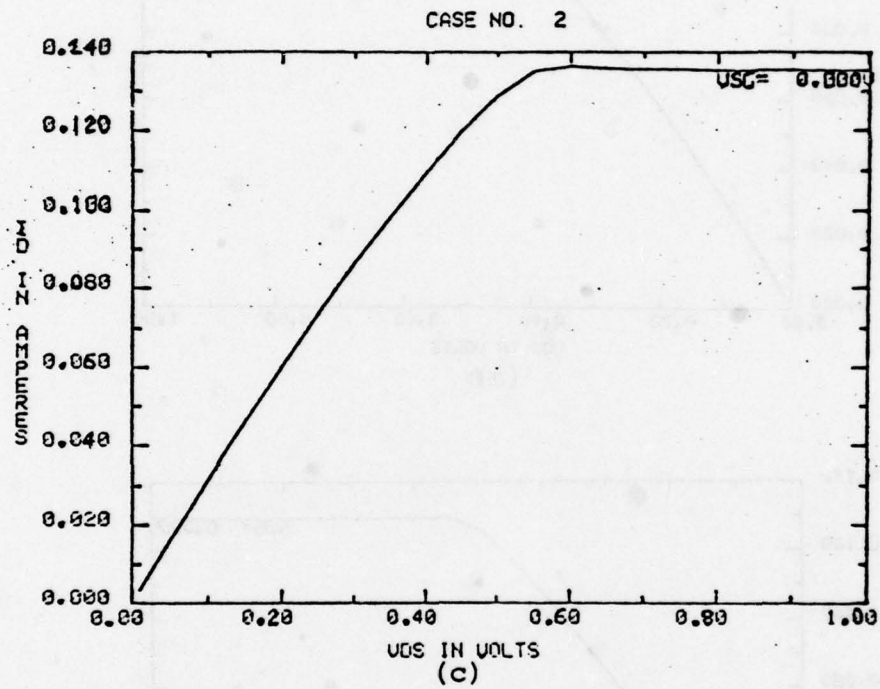


Figure 5.1 I-V curves of the FET
(c) 4 corrective iterations

It was further found that adding more than one iteration did not cause any appreciable change in the curves (see Figure 5.1(c) - 4 iterations). Thus it was decided to use one corrective iteration for mode A. Using the same procedure it was found that the necessary number of iterations for mode B is one, and for mode C is two.

5.3 CHARGE CORRECTION COEFFICIENTS

As described in chapter 3, the computer model employs a charge correction in operational mode A. This is a first order correction, which allows a small charge accumulation at the drain side of the gate active region (Equation 3-95). The procedure to set the coefficients CHAADR, CHADEX in Equation 3-95 is described in section 3.7.2. This procedure is demonstrated for the device considered here. The steps taken are as follows (all calculations were performed with the number of iterations as stated in the previous section):

- 1) choose $V_{DS}=3V$. This value is large enough compared to the "knee" ($\approx 0.5V$).

- 2) plot g_m versus V_{SG} for the above value of V_{DS} without charge correction (the two coefficients set to zero) - Figure 5.2(a).

- 3) set CHADEX=2 and plot g_m versus V_{SG} (with $V_{DS}=3V$) with CHAADR=0.2, 0.15, 0.1, 0.08. The "best" curve (according to section 3.7.2 guidelines) is for CHAADR=0.1 (Figure 5.2(b)).

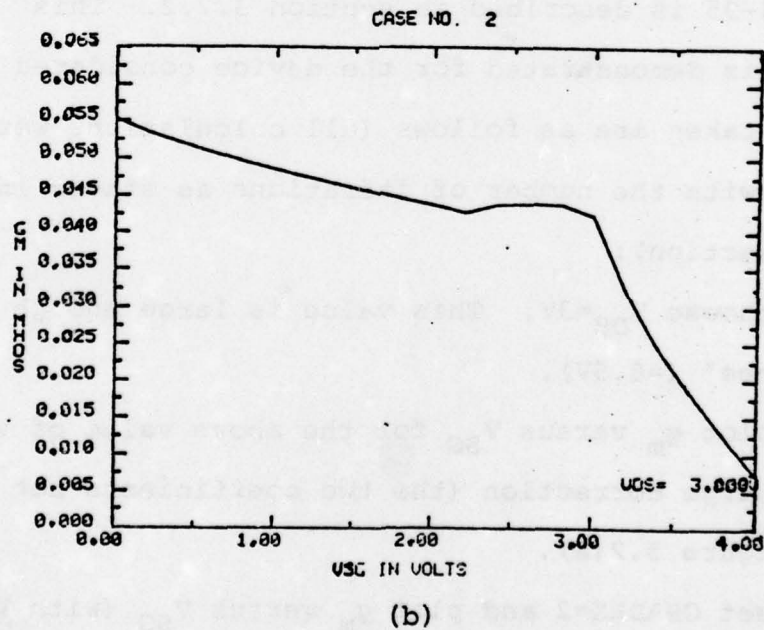
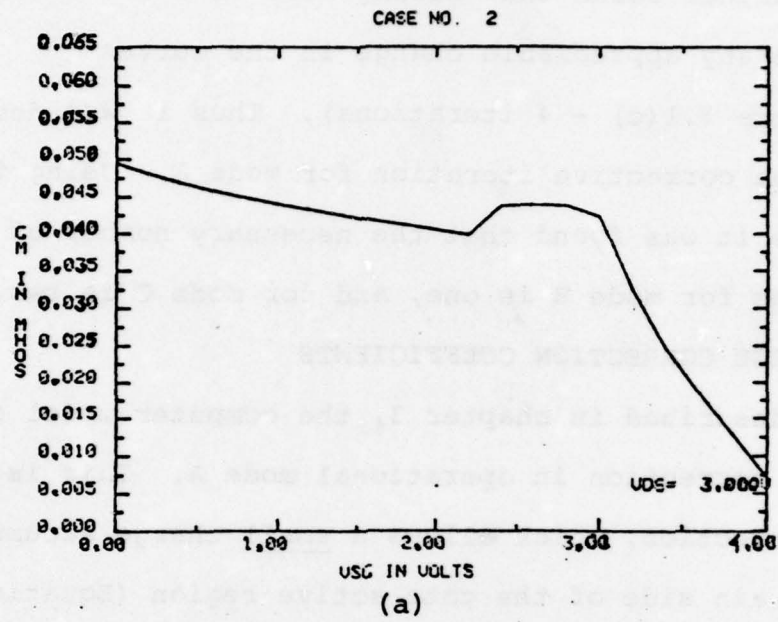


Figure 5.2 g_m plots (a) no charge correction
(b) CHAADR = 0.1, CHADEX = 2

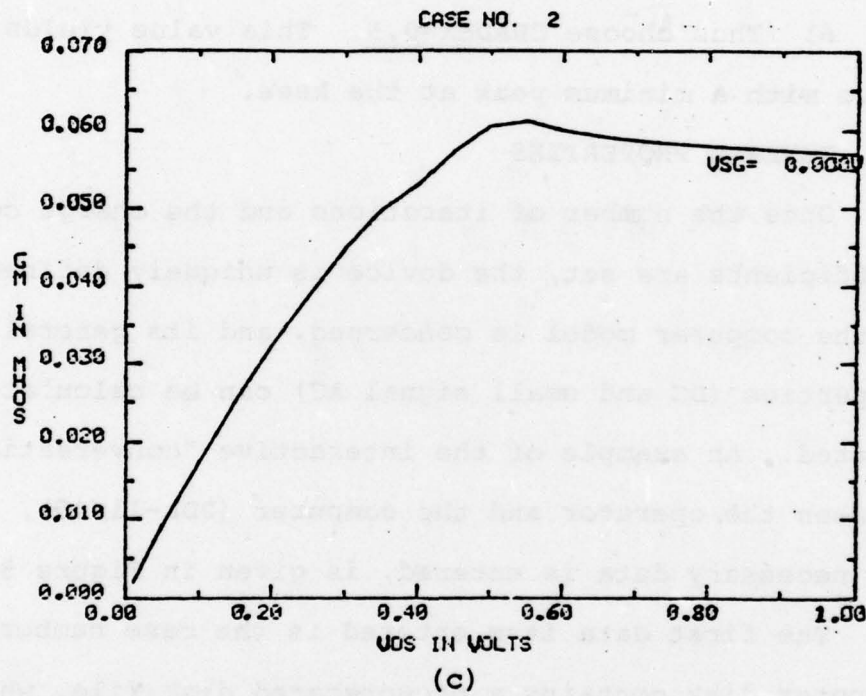


Figure 5.2 g_m plots (c) CHAADR = 0.1, CHADEX = 0.5

4) Thus choose CHAADR=0.1. This value yields a smooth curve for g_m with relatively small variation of g_m in modes A, B and a sharp decrease for mode C ($V_{SG} > 2.8V$).

5) set CHAADR=0.1 and plot g_m versus V_{DS} (with $V_{SG}=0$) with CHADEX=2, 1, 0.5, 0.3. The "best" curve (according to section 3.7.2 guidelines) is for CHADEX=0.5 (Figure 5.2(c)).

6) Thus choose CHADEX=0.5. This value yields a smooth curve with a minimum peak at the knee.

5.4 GENERAL PROPERTIES

Once the number of iterations and the charge correction coefficients are set, the device is uniquely defined as far as the computer model is concerned, and its general properties (DC and small signal AC) can be calculated and plotted. An example of the interactive "conversation" between the operator and the computer (PDP-11/45), in which the necessary data is entered, is given in Figure 5.3.

The first data item entered is the case number. The computer disk contains a pre-prepared disk file, which contains all the necessary information for a given device (Table 5.1). Each device is assigned a case number. Thus, when the case number is entered, the device parameters are read from the disk file. Next, the values of V_{DS} are entered (number of values, initial value, step). Likewise the values of V_{SG} . The frequency is entered only for the scattering parameters calculation. When no scattering

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INTERACTIVE MESFET ANALYSIS PACKAGE

IMAP READY: RUN
CASE NO.: 2
ASSIGN: NOVDS, VDSINI, AND VDSSTP= 31, 0., .05
ASSIGN: NOVSG, VSGINI, VSGSTP= 4, 0., 1.
ASSIGN: NOFRQ, FRQIN, FROSTP=
SPECIFY CHAADR, CHADEX: .1, .5
NUMBER OF ITERATIONS(VECTOR-9)? 1, 1, 2, 1, 1, 2, 1, 1, 2
PLOT THE RESULTS? YES
SCATTERING PARAMETERS OR CHARACTERISTICS? CH
WANT LINE PRINTER OUTPUT ALSO? NO

...WORKING

Figure 5.3 "Conversation" between operator
and computer PDP-11/45

parameters are calculated this data is item not needed. Next, the charge correction coefficients and the number of iterations are entered. The number of iterations vector, JJ, contains 9 components in the order as explained in section 4.5. Finally enter choices for plotting (yes or no), type of plotting (characteristics or scattering parameters), and line printer output (yes or no).

The results of the analysis corresponding to the "conversation" in Figure 5.3 is given in Figure 5.4(a). This Figure displays the I-V curves of the device for most of its dynamic range. More properties of the device are presented in Figure 5.4(b) and 5.5. Figure 5.4(b) displays the drain conduction current versus V_{SG} for a constant $V_{DS}=3V$. This Figure exhibits the linearity of the FET across most of its dynamic range. There is a great deviation from linearity as the device approaches cutoff (mainly in mode C - $V_{SG} > 3V$). The variation of the input capacitance with V_{SG} for $V_{DS}=3V$ is given in Figure 5.5(a). The capacitance is seen to be a monotonically decreasing function of V_{SG} . The drain conductance, g_d , is plotted in Figure 5.5(b) versus V_{DS} with $V_{SG}=1V$. It is seen to be quite large for low V_{DS} (high low-field mobility), but it decreases sharply above the knee.

For comparison, the I-V curves of the FET were computed using the Shockley model (see chapter 1). The results are presented in Figure 5.6. They were computed

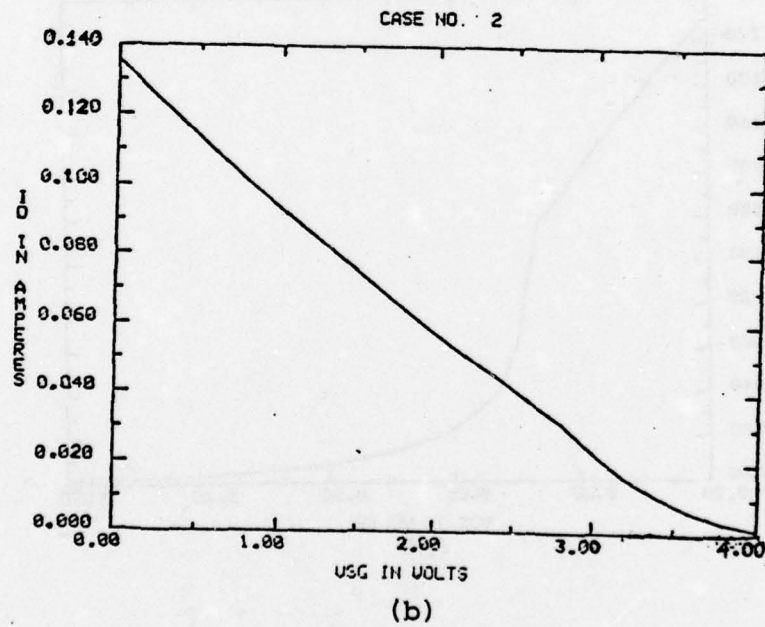
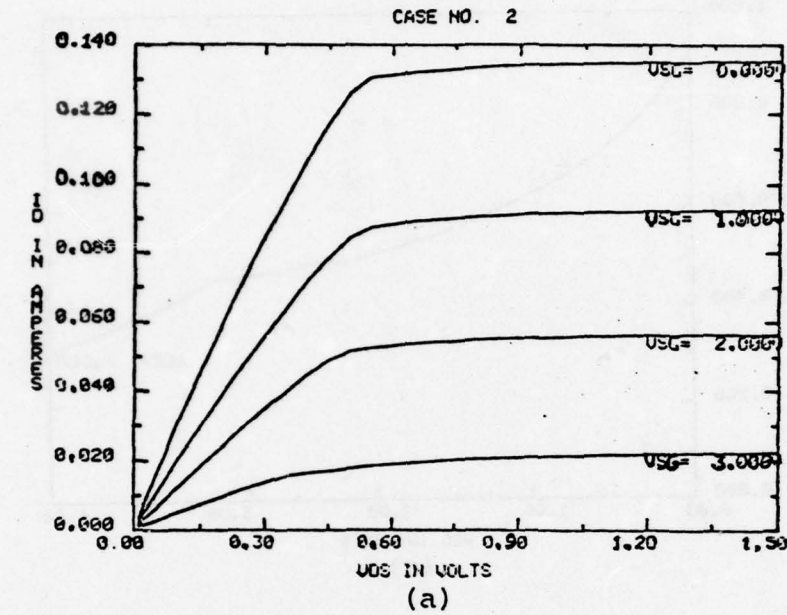


Figure 5.4 I-V curves of the FET (a) I_D vs. V_{DS}
(b) I_D vs. V_{SG}

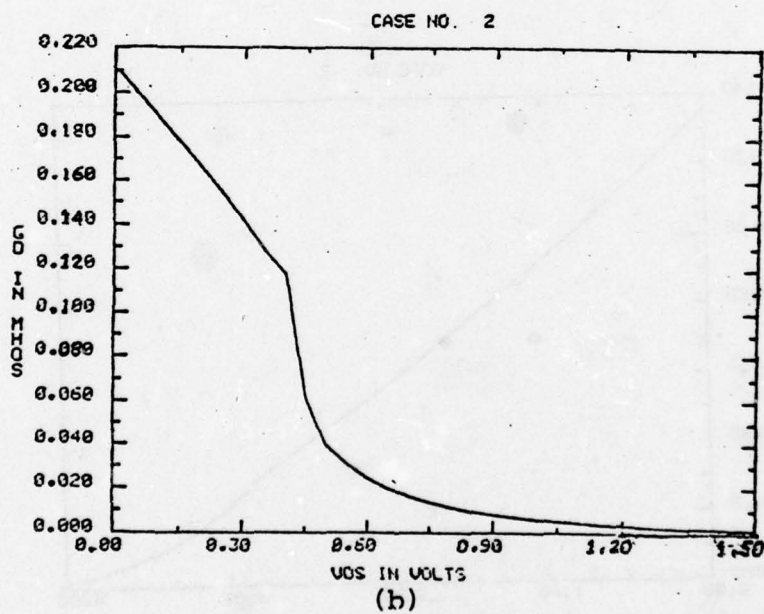
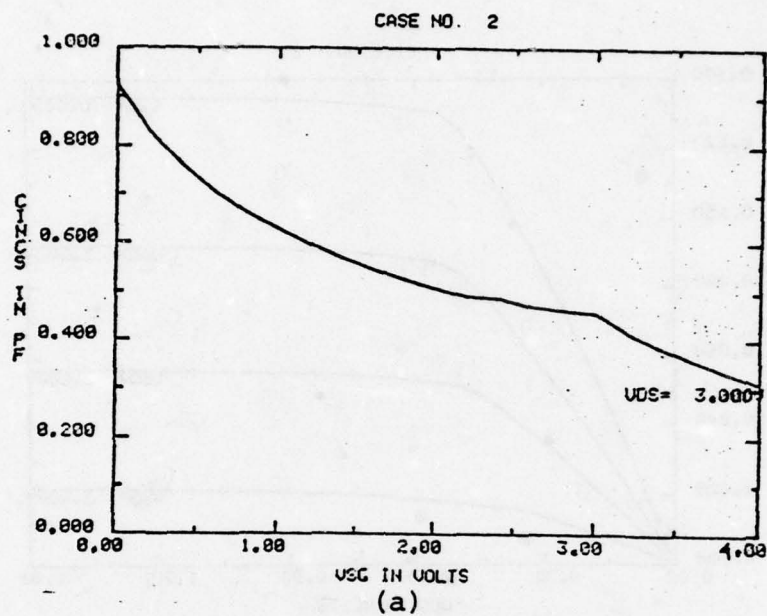


Figure 5.5 FET properties (a) input capacitance vs. V_{SG}
(b) drain conductance vs. V_{DS}

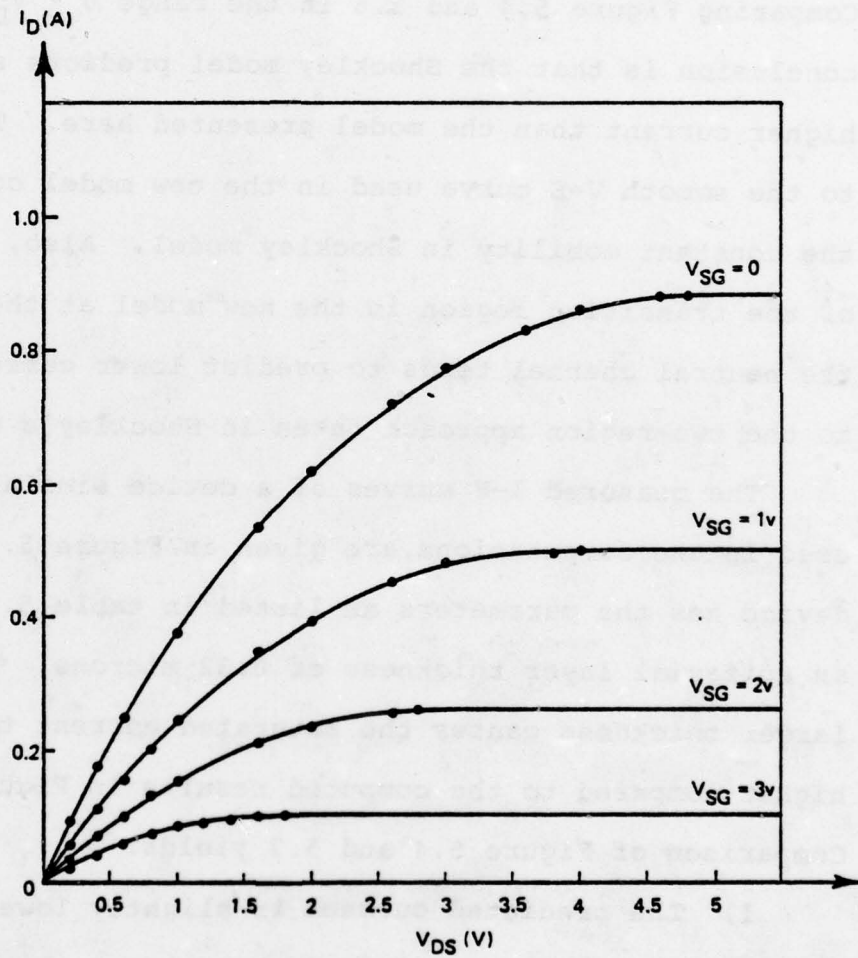


Figure 5.6 I-V curves for the FET using Shockley's model

using the low field mobility of GaAs ($4250 \text{ cm}^2/\text{V-sec}$) as the constant mobility for the Shockley model. The Shockley pinchoff voltage of this device is 4.88V, thus the currents predicted are very high. Of course, comparison can be done only for V_{DS} below the knee in Figure 5.4 ($\approx 0.45\text{V}$). Comparing Figure 5.4 and 5.6 in the range $0 \leq V_{DS} \leq 0.45$, the conclusion is that the Shockley model predicts somewhat higher current than the model presented here. This is due to the smooth V-E curve used in the new model compared to the constant mobility in Shockley model. Also, the existence of the transition region in the new model at the expense of the neutral channel tends to predict lower currents compared to the two-region approach taken in Shockley's model.

The measured I-V curves of a device similar to the one used in the computations are given in Figure 5.7. This device has the parameters as listed in table 5.1 except for an epitaxial layer thickness of 0.32 microns. The slightly larger thickness causes the saturated current to be somewhat higher compared to the computed results in Figure 5.4.

Comparison of Figure 5.4 and 5.7 yields:

- 1) The predicted current is slightly lower than the measured current, as explained above.
- 2) The predicted knee is lower than the measured knee. This fact is due to the fact that the external voltage in Figure 5.7 is compared to the internal voltage in

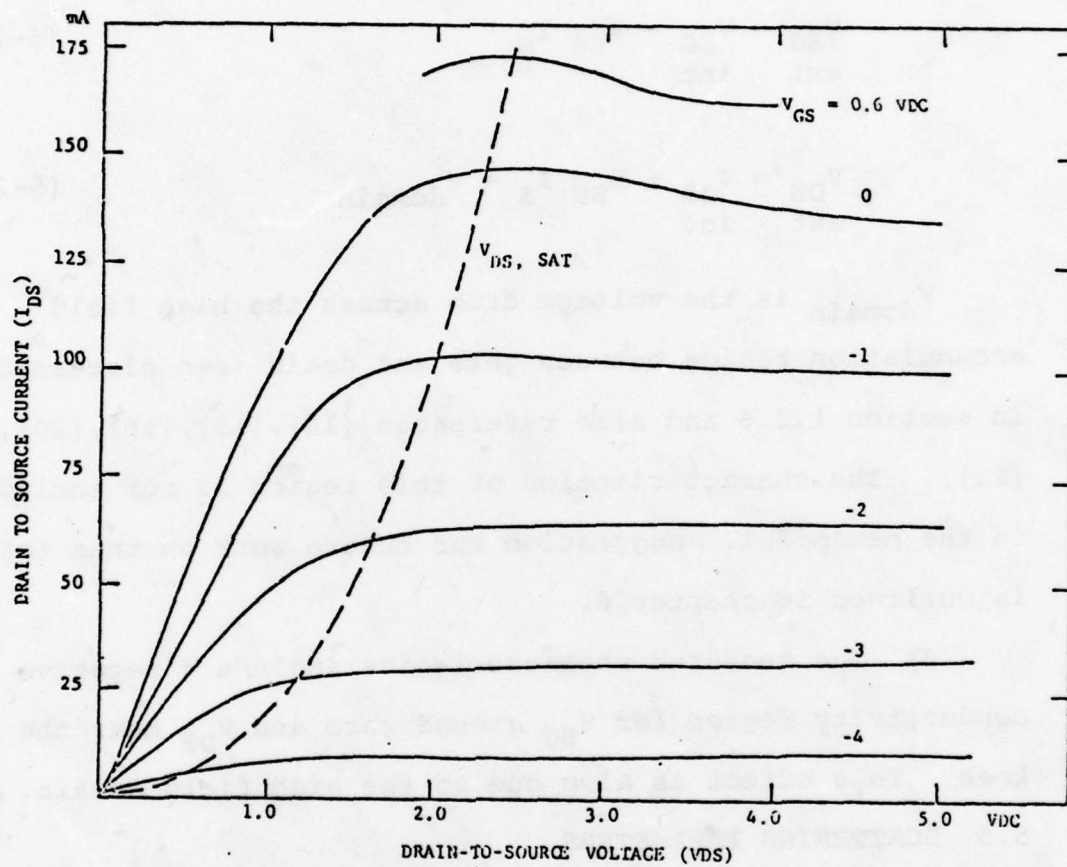


Figure 5.7 Measured I-V curves of the FET
(after Willing et al. [17])

Figure 5.4. To get the external voltages from the known internal voltages the voltage drop across the source and drain regions should be added:

$$V_{SG, ext} = V_{SG, int} - R_{SS} I_S \quad (5-1)$$

$$V_{DS, ext} = V_{DS, int} + R_{SS} I_S + V_{domain} \quad (5-2)$$

V_{domain} is the voltage drop across the high field accumulation region between gate and drain (see discussion in section 1.3.6 and also references [14],[15],[16],[20],[21]). The characterization of this region is not included in the new model. Suggestion for future work on this topic is outlined in chapter 6.

3) The measured characteristics include a negative conductivity region for V_{SG} around zero and V_{DS} near the knee. This effect is also due to the high field domain.

5.5 SCATTERING PARAMETERS

The most common method used to characterize a microwave linear two-part network is by its scattering parameters. When the FET is used as a small signal device, such as a low-noise amplifier, it is considered a linear device and can be characterized by its scattering parameters which relate the reflected (b_i) and incident (a_i) waves:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (5-3)$$

The measured scattering parameters of the device discussed in the previous section (with 0.32 micron epitaxial layer thickness) at bias $V_{SG}=2V$, $V_{DS}=6V$ are presented in Figure 5.8. S_{12} is quite small and ranges from 0.01 at 1GHz to 0.07 at 10 GHz (not shown).

The scattering parameters of the device given in Table 5.1 were calculated using the computer model. The general approach employed in the derivation of the small-signal parameters is a small perturbation around the DC bias. First, the general equations for the network in Figure 4.1 are considered. Then, each current and voltage is expressed as the sum of a DC value and a small AC term. This is inserted in the general equations above, and thus each equation is separated into DC and AC equations. For the small-signal parameter calculation only the AC equations are considered. In these equations express each variable in the form of amplitude and $e^{j\omega t}$ (i.e. $v_{SG}e^{j\omega t}$, $v_{ds}e^{j\omega t}$). Rearrange the resulting expressions into the standard form used for small-signal parameters definition (i.e. the external voltages

expressed in terms of the external current for the Z-matrix), and get the expressions for the parameters. For the network considered here (Figure 4.1) it was found useful to consider first a simplified network, and then add the additional elements. The procedure is as follows:

1) Consider the network as in Figure 4.1 excluding the elements L_g , L_d , C_{sin} , C_{so} , R_{subst} . The diode is excluded also since in small signal applications it is always off. The Z parameters of the simplified network are derived as discussed above. The results are:

$$Z_{11}^{(1)} = R_g + \frac{E \cdot D - C \cdot F}{A \cdot D - B \cdot C} \quad (5-4)$$

$$Z_{12}^{(1)} = \frac{A \cdot F - B \cdot E}{A \cdot D - B \cdot C} \quad (5-5)$$

$$Z_{21}^{(1)} = \frac{D \cdot G - C \cdot H}{A \cdot D - B \cdot C} \quad (5-6)$$

$$Z_{22}^{(1)} = R_{sd} + \frac{A \cdot H - B \cdot G}{A \cdot D - B \cdot C} \quad (5-7)$$

where:

$$A = -j\omega \cdot GVSG \quad (5-8)$$

$$B = -j\omega \cdot GVDS \quad (5-9)$$

$$C = -g_m \cos(\omega\tau) + j(\omega \cdot \text{DVSG} + g_m \sin(\omega\tau)) \quad (5-10)$$

$$D = g_d + j\omega \cdot \text{DVDS} \quad (5-11)$$

$$E = -(1 + g_m R_{ss} \cos(\omega\tau)) + j[\omega \cdot \text{SVSG}(R_c + R_{ss}) + g_m R_{ss} \sin(\omega\tau)] \quad (5-12)$$

$$F = g_d R_{ss} + j\omega \cdot \text{SVDS} \cdot (R_c + R_{ss}) \quad (5-13)$$

$$G = -g_m R_{ss} \cos(\omega\tau) + j[\omega R_{ss} \cdot \text{SVSG} + g_m R_{ss} \sin(\omega\tau)] \quad (5-14)$$

$$H = 1 + g_d R_{ss} + j\omega \cdot R_{ss} \cdot \text{SVDS} \quad (5-15)$$

τ is the time delay (transit time). The Z parameters equations were first derived without considering τ , and then instead of g_m the expression $g_m e^{j\omega\tau}$ was used, thus yielding the above expressions.

2) Add to the network considered in step 1 the resistor R_{subst} . Since this resistor is parallel to the output it directly adds to $Y_{22}^{(1)}$. Thus, calculate the inverse of the $Z^{(1)}$ -matrix to find the $Y^{(1)}$ matrix, and add $1/R_{\text{subst}}$ to $Y_{22}^{(1)}$, yielding the $Y^{(2)}$ matrix.

3) Add to the network considered in step 2 the 3 inductances: L_g , L_s , L_d . Since the inductors are in series with the terminals of network 2 it is easy to show (after converting $Y^{(2)}$ into $Z^{(2)}$):

$$Z_{11}^{(3)} = Z_{11}^{(2)} + j\omega(L_g + L_s) \quad (5-16)$$

$$Z_{12}^{(3)} = Z_{12}^{(2)} + j\omega L_s \quad (5-17)$$

$$Z_{21}^{(3)} = Z_{21}^{(2)} + j\omega L_s \quad (5-18)$$

$$Z_{22}^{(3)} = Z_{22}^{(2)} + j\omega(L_D + L_s) \quad (5-19)$$

4) Add to the network considered in step 3 the 2 capacitors: C_{sin} , C_{so} , thus yielding the final network. As in step 2, here too the capacitors admittances add directly to $Y_{11}^{(3)}$, $Y_{22}^{(3)}$, respectively:

$$Y_{11}^{(4)} = Y_{11}^{(3)} + j\omega C_{sin} \quad (5-20)$$

$$Y_{12}^{(4)} = Y_{12}^{(3)} \quad (5-21)$$

$$Y_{21}^{(4)} = Y_{21}^{(3)} \quad (5-22)$$

$$Y_{22}^{(4)} = Y_{22}^{(3)} + j\omega C_{so} \quad (5-23)$$

Thus, by successive transformations from Z to Y and Y to Z the parameters of the assembled FET chip are derived. The Y parameters computed by Equations (5-20) to (5-23) are used to calculate the scattering parameters by the standard transformation equations (see [24]):

$$S_{11} = \frac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}} \quad (5-24)$$

$$S_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}} \quad (5-25)$$

$$S_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}} \quad (5-26)$$

$$S_{22} = \frac{(1+y_{11})(1-y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}} \quad (5-27)$$

where y_{11} , y_{12} , y_{21} , y_{22} are the normalized Y parameters, namely, the Y parameters divided by $Y_0 (=1/Z_0)$.

The calculated scattering parameters of the device considered here (Table 5.1) for applied DC bias of $V_{DS}=5.8V$, $V_{SG}=2.1V$ (internal voltages - as discussed in section 5.4) are presented in Figure 5.8 for the frequency range 1-10 GHz. Comparing the calculated and measured parameters one concludes that there is a reasonable agreement for S_{11} (the increased difference in the high frequency may be due to inaccuracy in the assumed

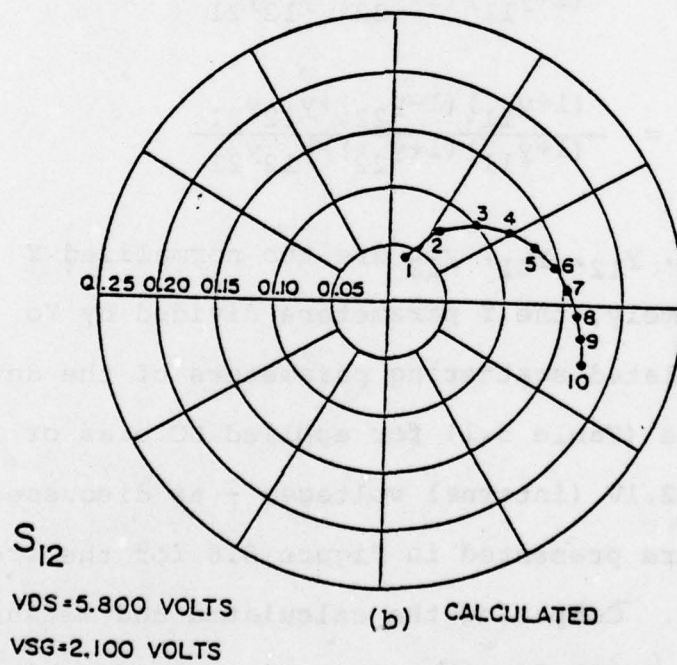
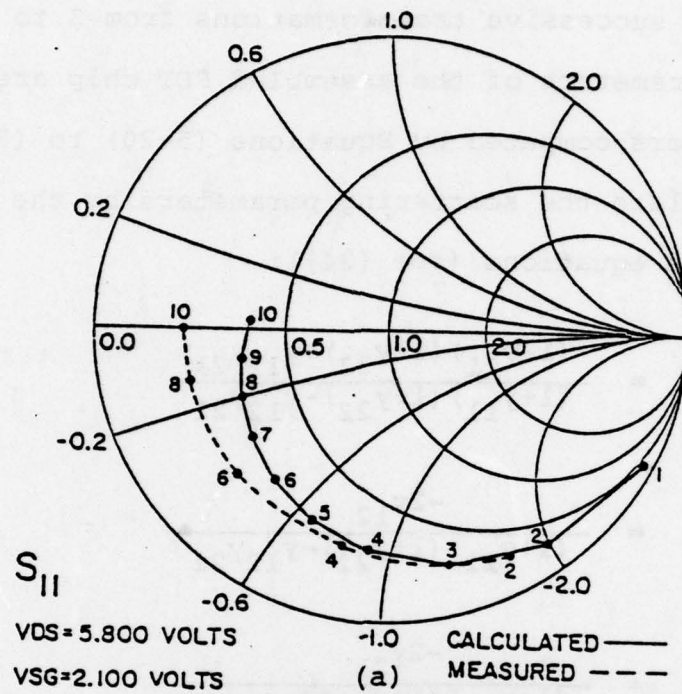


Figure 5.8 Scattering parameters of the FET
(a) S_{11} (b) S_{12} (frequency in GHz)

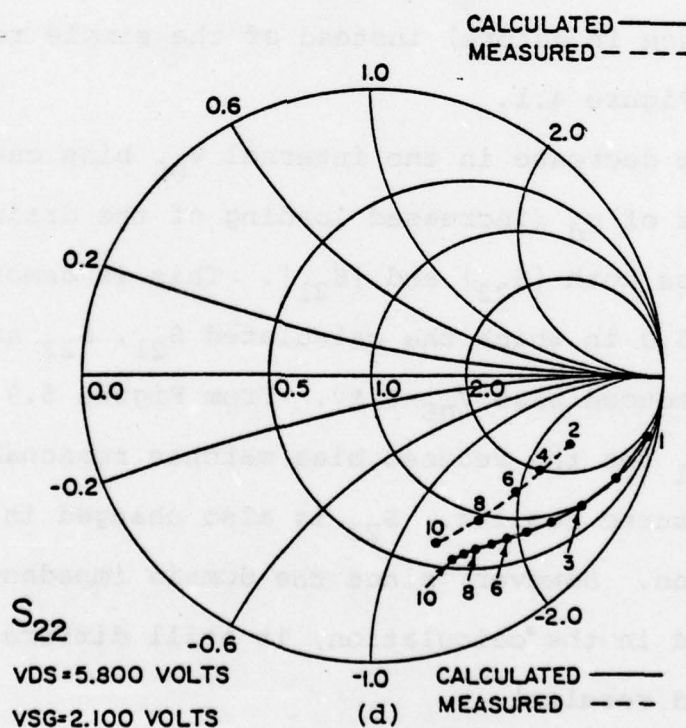
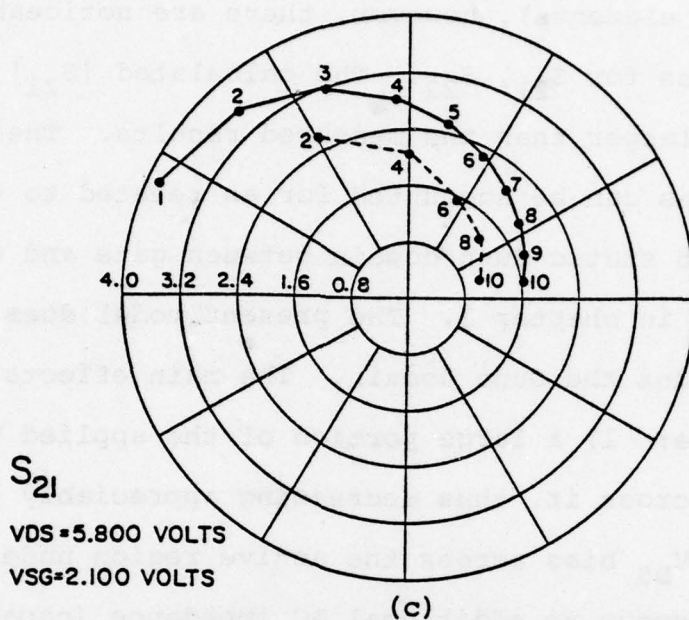


Figure 5.8 Scattering parameters of the FET
(c) S_{21} (d) S_{22} (frequency in GHz)

parasitic elements), however, there are noticeable differences for S_{21} , S_{22} . The calculated $|S_{21}|$, $|S_{22}|$ are somewhat larger than the measured results. These differences can be accounted for as related to the high-field static Gunn domain between gate and drain, as discussed in chapter 1. The present model does not take into account the Gunn domain. The main effects of the domain are: 1) a large portion of the applied V_{DS} bias is dropped across it, thus decreasing appreciably the internal V_{DS} bias across the active region under the gate. 2) it presents an additional AC impedance (capacitance and resistance in nature) instead of the simple resistance R_{sd} in Figure 4.1.

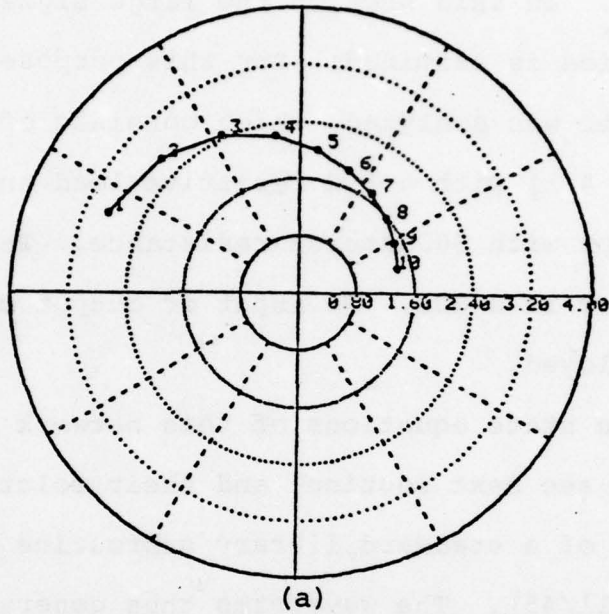
The decrease in the internal V_{DS} bias causes an increase of g_d (increased loading of the drain), which decreases both $|S_{22}|$ and $|S_{21}|$. This is demonstrated in Figure 5.9 in which the calculated S_{21} , S_{22} are presented for a reduced bias $V_{DS}=0.8V$. From Figure 5.9 it is seen that S_{21} for the reduced bias matches reasonably with the measured results. S_{22} is also changed in the correct direction. However, since the domain impedance is not included in the calculation, it still differs from the measured results.

5.6 LARGE SIGNAL ANALYSIS

The preceeding section compares the calculated DC and small signal performance of the FET with experimental

S21
CASE NO. 2

UDS= 0.800 VOLTS
USG= 2.100 VOLTS
(RMAX= 4.000)



S22
CASE NO. 2

UDS= 0.800 VOLTS
USG= 2.100 VOLTS

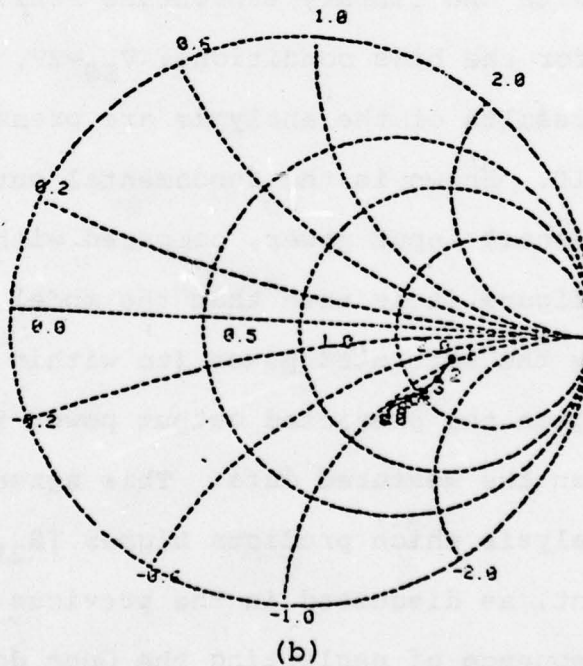


Figure 5.9 Scattering parameters for reduced bias
(a) S_{21} (b) S_{22} (frequency in GHz)

results. In this section the large signal performance of the device is examined. For this purpose, a simple power amplifier was analyzed, which consists of the FET (Figure 4.1) with a 50Ω resistive load and an ideal voltage generator with 50Ω source resistance. The operating frequency is 2 GHz. No input or output matching networks are employed.

The state equations of this network were derived (for details see next section) and their solution obtained with the use of a standard library subroutine RKGS (SSP library of PDP-11/45). The waveforms thus generated, were Fourier analyzed with the library subroutine FORIT. The analysis was done for the bias conditions: $V_{SG}=2V$, $V_{DS}=6V$.

The results of the analysis are presented in Figure 5.10. Shown is the fundamental output power versus the fundamental input power, compared with measured data. From the figure it is seen that the model predicts quite accurately the saturated power (to within 0.4db). In the linear region the predicted output power is about 1.5db higher than the measured data. This agrees with the small signal analysis which predicts higher $|S_{21}|$ than the measurement, as discussed in the previous section. This is a consequence of neglecting the Gunn domain in the model.

Since the results obtained for the DC, small signal, and large signal analysis are reasonable and fairly close

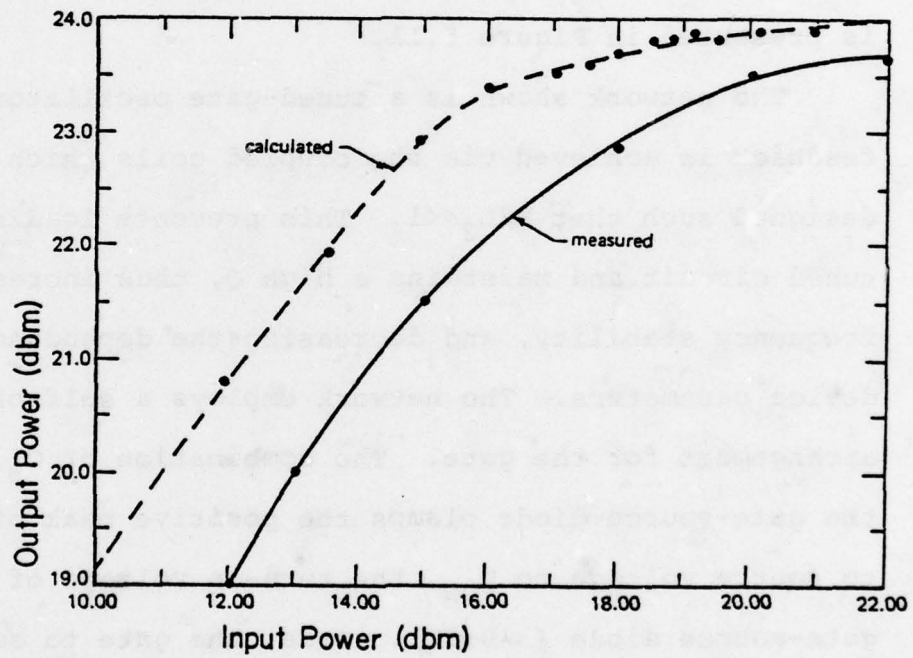


Figure 5.10 Saturation characteristic of the FET
($V_{SG} = 2\text{v}$, $V_{DS} = 6\text{v}$)

to the measurement data, we may turn now, with some confidence, to the application of the model to a practical large signal network.

5.7 OSCILLATOR ANALYSIS

To demonstrate the use of the model in a large signal case, an oscillator structure was analyzed and its properties evaluated. The network considered is suggested by Clarke and Hess (page 241 in [23]). The circuit diagram is presented in Figure 5.11.

The network shown is a tuned-gate oscillator. The feedback is achieved via the coupled coils which are designed such that $M/L_2 \ll 1$. This prevents loading of the tuned circuit and maintains a high Q , thus increasing the frequency stability, and decreasing the dependence on device parameters. The network employs a self-bias arrangement for the gate. The combination of C_B , R_B and the gate-source diode clamps the positive peak of the gate to source voltage to V_{ON} , the turn-on voltage of the gate-source diode ($\approx 0.5V$). Thus, the gate to source bias is automatically set to approximately the negative of the oscillation amplitude, which is a self-limiting mechanism.

An attempt was made to design a 2GHz oscillator, using the guidelines of Clarke and Hess [23], and then analyze it in the time domain using the FET model, starting at $t=0$ (turn-on of V_{DD}) up to the point at which steady

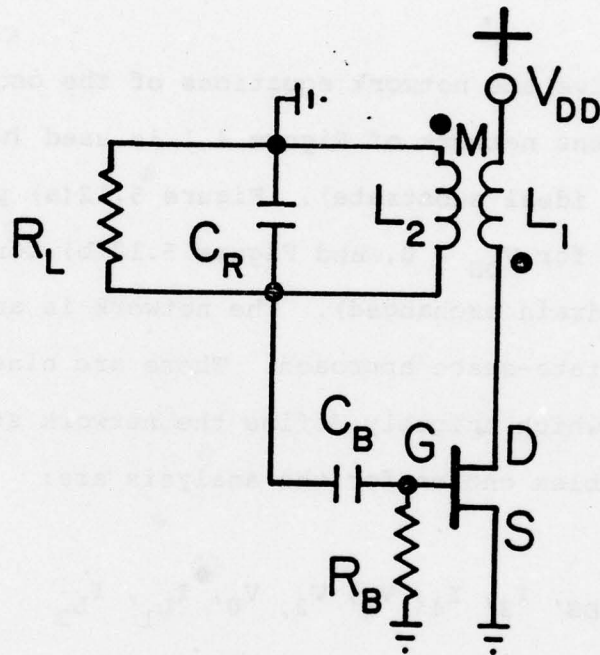


Figure 5.11 Oscillator network

state is reached. The component values chosen are (design number 1):

$$V_{DD}=6V, L_1=L_2=1 \text{ nHy}, M=0.2 \text{ nHy}, C_R=5.5\text{pF},$$

$$R_L=1k\Omega, C_B=10\text{pF}, R_B=3K\Omega$$

To derive the network equations of the oscillator, the FET equivalent network of Figure 4.1 is used (with $R_{\text{subst}} = \infty$ - ideal substrate). Figure 5.12(a) presents the network for $V_{DS} > 0$, and Figure 5.12(b) for $V_{DS} < 0$ (source and drain exchanged). The network is analyzed using the state-space approach. There are nine state variables, which uniquely define the network status. The state variables chosen for the analysis are:

$$V_{SG}, V_{DS}, I_3, I_4, V_1, V_2, V_0, I_{L_1}, I_{L_2}$$

Note that the variables V_{SG}, V_{DS} are different in the two networks in Figure 5.12. In (a) they are designated by superscript S, and in (b) by superscript D. Since the difference in V_{DS} is just in $(V_{DS}^{(D)} = -V_{DS}^{(S)})$ it does not present a problem, and the variable $V_{DS}^{(S)}$ was chosen as the state variable for both

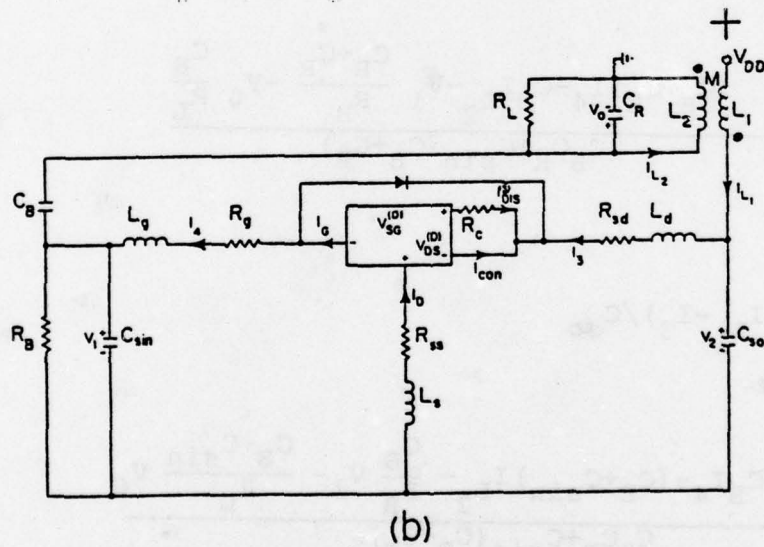
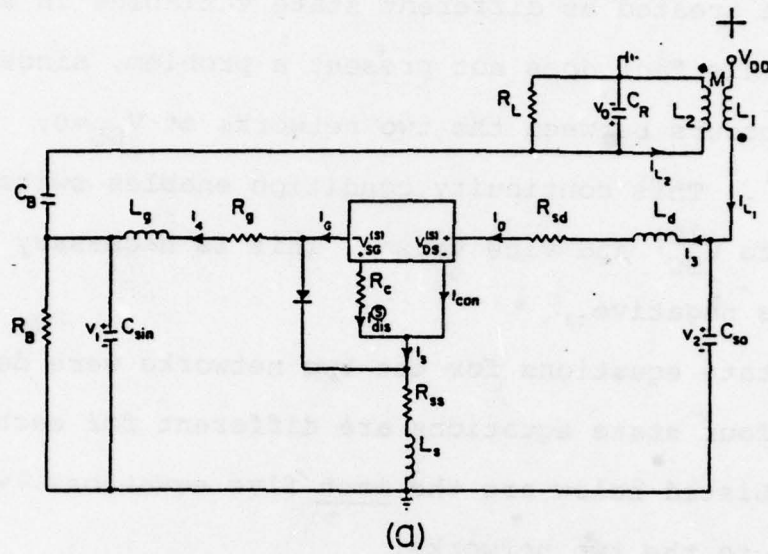


Figure 5.12 Oscillator equivalent network
(a) $V_{DS} > 0$ (b) $V_{DS} < 0$

networks. However, $V_{SG}^{(S)}$ and $V_{SG}^{(D)}$ are entirely different, and must be treated as different state variables in each network. This fact does not present a problem, since when switching occurs between the two networks at $V_{DS}=0$, $V_{SG}^{(S)} = V_{SG}^{(D)}$. This continuity condition enables switching from $V_{SG}^{(S)}$ to $V_{SG}^{(D)}$ and vice versa. This is necessary if V_{DS} becomes negative.

The state equations for the two networks were derived. The first four state equations are different for each network. Listed below are the last five equations, which are common to the two networks:

$$\textcircled{5} \quad \frac{dV_1}{dt} = \frac{(C_B + C_R)I_4 - C_B I_{L_2} - V_1 \frac{C_B + C_R}{R_B} - V_0 \frac{C_B}{R_L}}{C_B C_R + C_{\sin}(C_B + C_R)} \quad (5-28)$$

$$\textcircled{6} \quad \frac{dV_2}{dt} = (I_{L_1} - I_3)/C_{so} \quad (5-29)$$

$$\textcircled{7} \quad \frac{dV_0}{dt} = \frac{C_B I_4 - (C_B + C_{\sin})I_{L_2} - \frac{C_B}{R_B} V_1 - \frac{C_B + C_{\sin}}{R_L} V_0}{C_B C_R + C_{\sin}(C_B + C_R)} \quad (5-30)$$

$$\textcircled{8} \quad \frac{dI_{L_1}}{dt} = \frac{L_2(V_{DD} - V_2) - M V_0}{L_1 L_2 - M^2} \quad (5-31)$$

$$\textcircled{9} \quad \frac{dI_{L2}}{dt} = \frac{L_1 V_0 - M(V_{DD} - V_2)}{L_1 L_2 - M^2} \quad (5-32)$$

The first four state equations for the case $V_{DS} > 0$ (Figure 5.12(a)) are as follows:

$$\textcircled{1} \quad \frac{dv_{SG}^{(S)}}{dt} = \frac{GVDS(I_3 - I_{con}) - DVDS I_G}{GVDS \cdot DVSG - DVDS \cdot GVSG} \quad (5-33)$$

$$\textcircled{2} \quad \frac{dv_{DS}^{(S)}}{dt} = \frac{GVSG(I_3 - I_{con}) - DVSG I_G}{DVDS \cdot GVSG - GVDS \cdot DVSG} \quad (5-34)$$

where: $I_G = I_4$ for diode OFF

$$I_G = I_3 - I_{con} - \frac{v_{SG}^{(S)} + v_{ON}}{R_C} \quad \text{for diode ON} \quad (5-35)$$

The diode state is determined by comparing the diode voltage against v_{ON} :

$$v_{DIODE} = -v_{SG}^{(S)} + R_C(I_3 - I_4 - I_{con}) \quad (5-36)$$

The third and fourth equations are:

DIODE OFF

$$\textcircled{3} \frac{dI_3}{dt} = \frac{(L_g + L_s) (V_2 - V_{DS})^{(S)} - L_s (V_{SG} + V_1 + R_c I_{con})^{(S)} - I_3 [(L_s + L_g) (R_{sd} + R_{ss}) - L_s (R_{ss} + R_c)] + I_4 [R_{ss} L_g - L_s (R_g + R_c)]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-37)$$

$$\textcircled{4} \frac{dI_4}{dt} = \frac{L_s (V_2 - V_{DS})^{(S)} - (L_d + L_s) (V_{SG} + V_1 + R_c I_{con})^{(S)} - I_3 [L_s (R_{sd} + R_{ss}) - (L_d + L_s) (R_{ss} + R_c)] + I_4 [R_{ss} L_s - (L_d + L_s) (R_g + R_{ss} + R_c)]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-38)$$

DIODE ON

$$\textcircled{1} \frac{dI_3}{dt} = \frac{(L_s + L_g) (V_2 - V_{DS})^{(S)} - L_s (V_1 - V_{OH})^{(S)} + I_3 [L_s R_{ss} - (L_s + L_g) (R_{sd} + R_{ss})] + I_4 [L_g R_{ss} - L_s R_g]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-39)$$

$$\textcircled{1} \frac{dI_4}{dt} = \frac{L_s^{(S)} (V_2 - V_{DS}) - (L_s + L_d) (V_1 - V_{ON}) + I_3 [L_d R_{ss} - L_s R_{sd}] + I_4 [L_s R_{ss} - (L_s + L_d) (R_g + R_{ss})]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-40)$$

The first four state equations for the case of $V_{DS} < 0$ (Figure 5.12(b)) are as follows:

$$\textcircled{1} \frac{dV_{SG}^{(D)}}{dt} = \frac{GVDS (I_D - I_{con}) - DVDS \cdot I_G}{GVDS \cdot DVSG - DVDS \cdot GVSG} \quad (5-41)$$

$$\textcircled{2} \frac{dV_{DS}^{(S)}}{dt} = \frac{GVSG (I_D - I_{con}) - DVSG \cdot I_G}{GVDS \cdot DVSG - DVSD \cdot GVSG} \quad (5-42)$$

$$\text{where:} \quad I_D = I_4 - I_3 \quad (5-43)$$

$$I_G = I_4 \quad \text{for diode OFF} \quad (5-44)$$

$$I_G = I_4 - I_3 - I_{con} - \frac{V_{SG}^{(D)} + V_{ON}}{R_C} \quad \text{for diode ON} \quad (5-45)$$

$$V_{DIODE}^{(D)} = -V_{SG} - R_C (I_3 + I_{con}) \quad (5-46)$$

The third and fourth equations are:

Diode OFF

$$\textcircled{3} \frac{dI_3}{dt} = \frac{(L_s + L_g) (V_2 - V_{DS}^{(S)}) - L_s (V_1 + V_{SG}^{(D)}) + R_c I_{con} - V_{DS}^{(S)} - I_3 [(L_s + L_g) (R_{sd} + R_{ss}) + L_s (R_c - R_{ss})] + I_4 [R_{ss} L_g - L_s R_g]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-47)$$

$$\textcircled{4} \frac{dI_4}{dt} = \frac{L_s (V_2 - V_{DS}^{(S)}) - (L_s + L_d) (V_1 + V_{SG}^{(D)}) + R_c I_{con} - V_{DS}^{(S)} - I_3 [L_s (R_{sd} + R_{ss}) + (L_s + L_d) (R_c - R_{ss})] + I_4 [L_s R_{ss} - (L_s + L_d) (R_g + R_{ss})]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-48)$$

Diode ON

$$\textcircled{3} \frac{dI_3}{dt} = \frac{(L_g + L_s) (V_2 - V_{DS}^{(S)}) - L_s (V_1 - V_{DS}^{(S)} - V_{ON}) - I_3 [R_{sd} + R_{ss}] (L_g + L_s) - L_s R_{ss}}{L_d L_s + L_d L_g + L_s L_g} + I_4 [R_{ss} L_g - R_g L_s] \quad (5-49)$$

$$\textcircled{4} \frac{dI_4}{dt} = \frac{L_s (V_2 - V_{DS}^{(S)}) - (L_s + L_d) (V_1 - V_{DS}^{(S)} - V_{ON}) - I_3 [L_s (R_{sd} + R_{ss}) - (L_s + L_d) R_{ss}] + I_4 [L_s R_{ss} - (L_s + L_d) (R_{ss} + R_g)]}{L_d L_s + L_d L_g + L_s L_g} \quad (5-50)$$

In the above equations (5-33 to 5-50) the various circuit element values are given, and the other parameters (G_{VDS} , D_{VDS} , R_c , I_{con} , etc) are evaluated by the FET model for the given pair of (V_{SG} , V_{DS}) in the case of $V_{DS} > 0$, and for the pair (V_{SG} , $-V_{DS}$) in the case of $V_{DS} < 0$.

The above set of state equations is solved numerically on a digital computer. The computer used is a mini computer PDP-11/45, and the library subroutine used to solve the equations is called RKGS. The solution is based on the Runge-Kutta algorithm. For the specific problem outlined above the initial conditions for the state variables are all zero at $t=0$. At $t=0$ the bias voltage V_{DD} is applied and the oscillation build-up starts. The computations were performed up to $t=50\text{nsec}$ (100 cycles at the oscillation frequency of 2 GHz), at which point the oscillator has practically reached steady state.

Figure 5.13 presents the build up process of the oscillator. Shown is the output voltage, V_0 , as a function of time. It grows from zero at $t=0$ to an amplitude of approximately 7 volts after about 80 cycles (40nsec). A two cycles period of the output voltage in steady state (91st and 92nd cycles) is given in Figure 5.14. It is seen that the output waveform is practically distortion free. This waveform was Fourier analyzed using a standard library subroutine, FORIT, in the mini computer PDP-11/45.

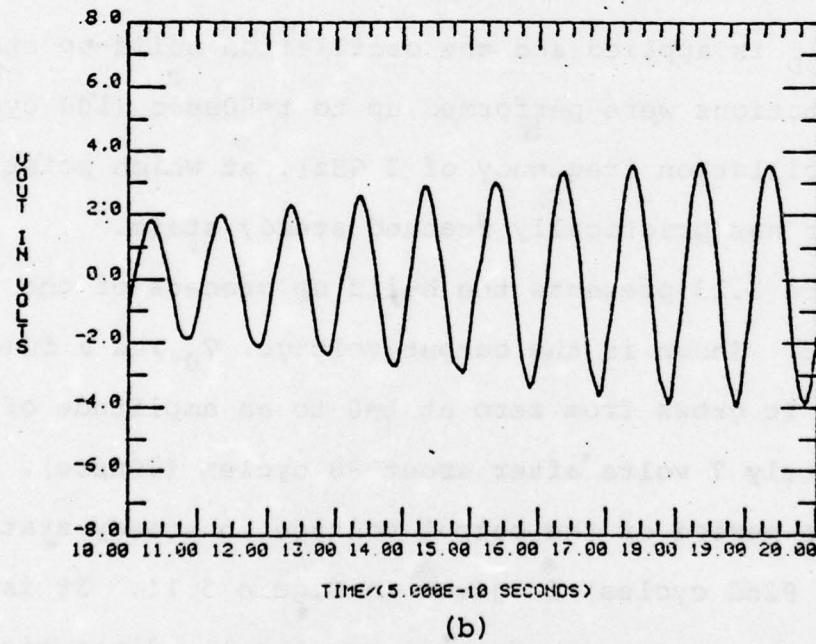
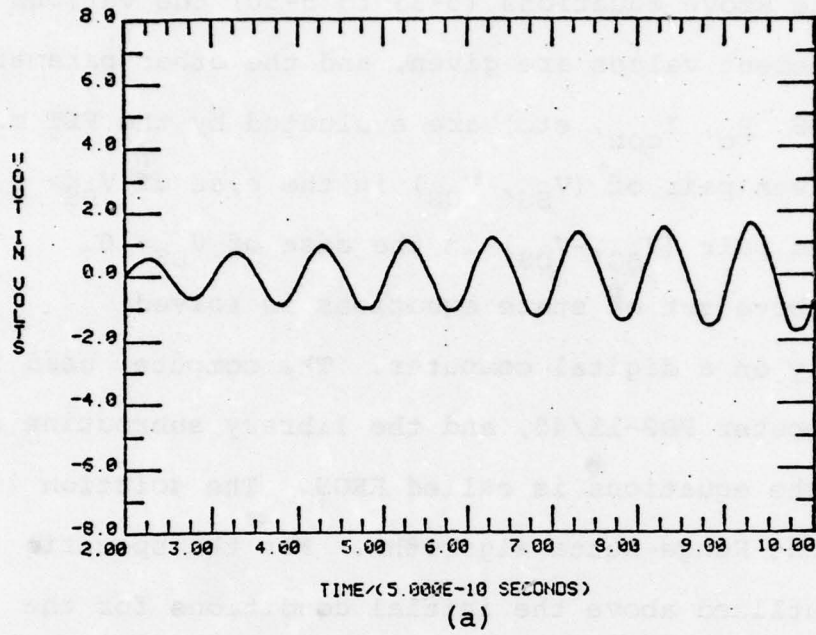
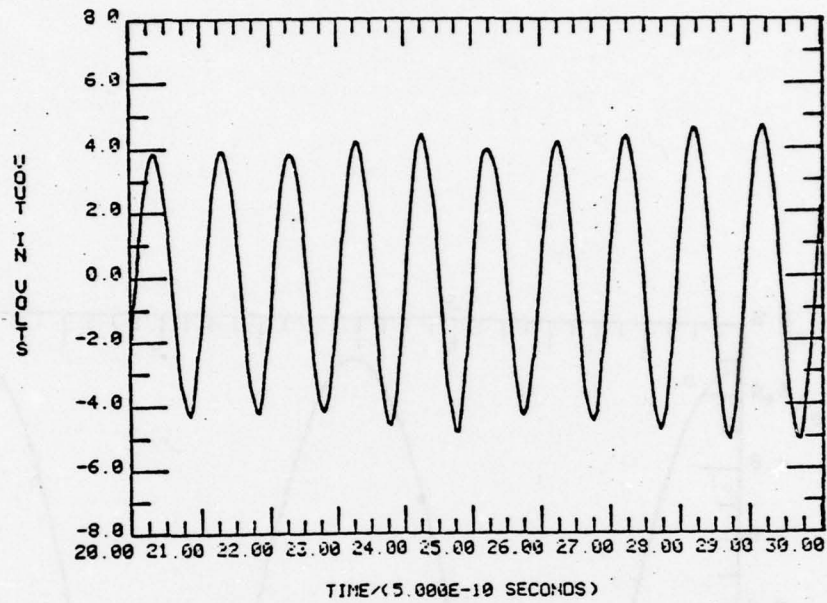
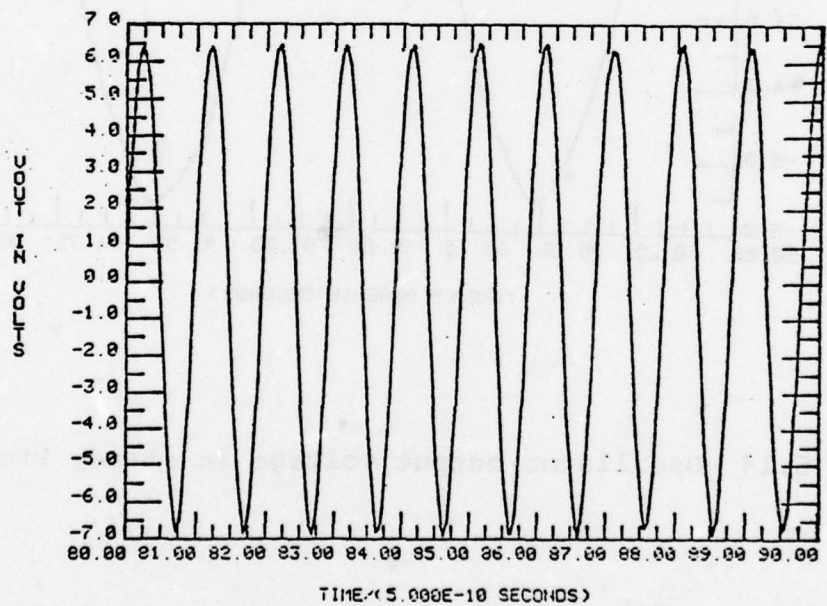


Figure 5.13 Oscillator build-up (a) 3rd to 10th cycles
(b) 11th to 20th cycles



(c)



(d)

Figure 5.13 Oscillator build-up (c) 21st to 30th cycles
(d) 81st to 90th cycles

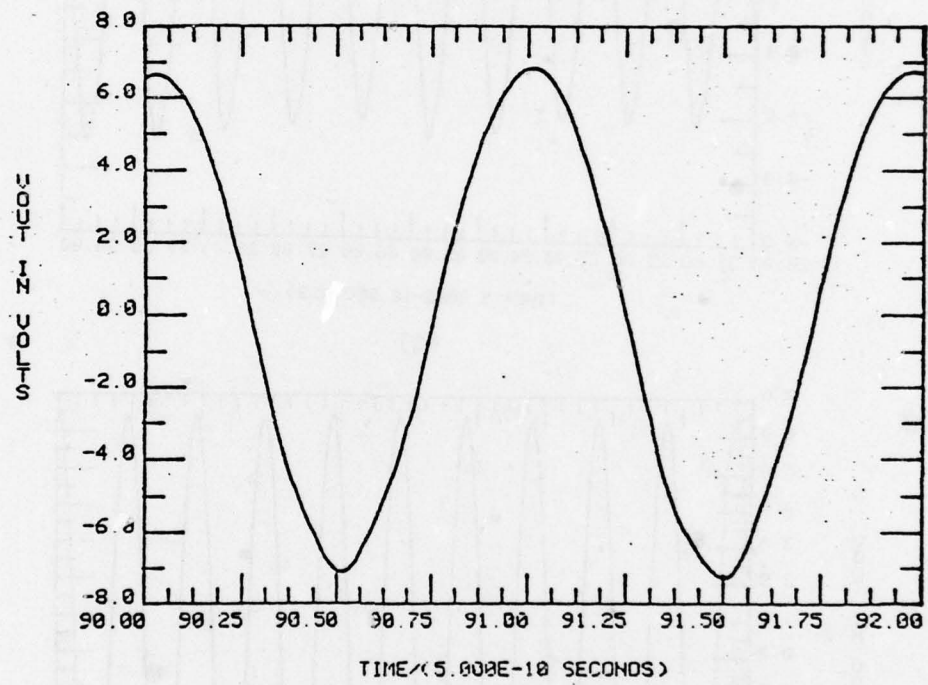


Figure 5.14 Oscillator output voltage in steady state

The results of the Fourier analysis confirm the visual impression of Figure 5.14. The fundamental output power is 24.3 mW (13.9 dbm). The second harmonic power is 0.035 mW (-14.6dbm), namely, 28.5 db below the fundamental. The other harmonics are even lower than the second (i.e. the third harmonic is -21.6dbm). The total DC power supplied by the DC source V_{DD} is 245 mW. Thus, the oscillator efficiency is about 10%.

There are two problems with the oscillator circuit considered here: 1) There exists a low frequency parasitic oscillation in addition to the desired oscillation at 2 GHz. This low frequency oscillation modulates the amplitude of the output waveform. This can be seen in Figure 5.13(d), in which the "peaks" of the output sine wave are seen to vary slightly from one cycle to another. The modulation frequency can be roughly estimated as 250-300 MHz. The amount of amplitude modulation is quite small. The peak-to-peak change of the carrier amplitude is about 0.17 V (compared to 7V amplitude). 2) There exists high frequency parasitic oscillations in the drain circuit. This can be seen in the waveforms of V_{DS} and I_d , presented in Figure 5.15 and 5.16. The high frequency oscillations do not appear in the output waveform due to the filtering effect of the resonant circuit. The frequency of these parasitic oscillations can be estimated at about 10 GHz.

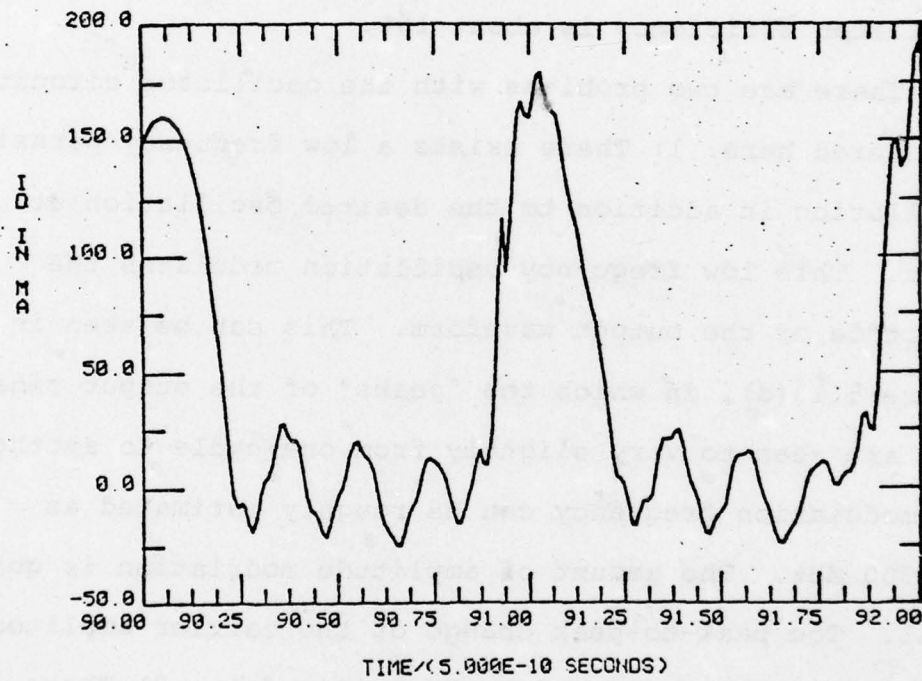


Figure 5.15 Drain current waveform

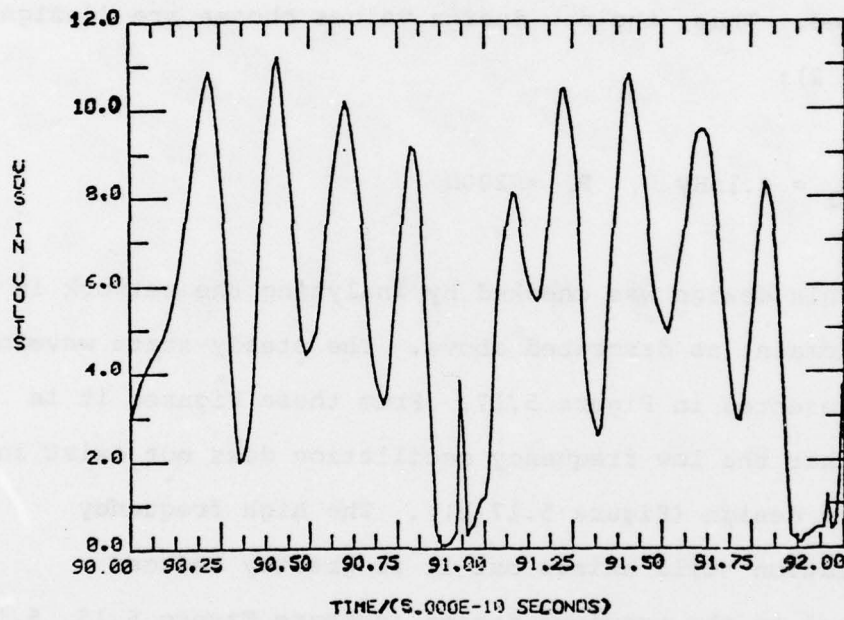


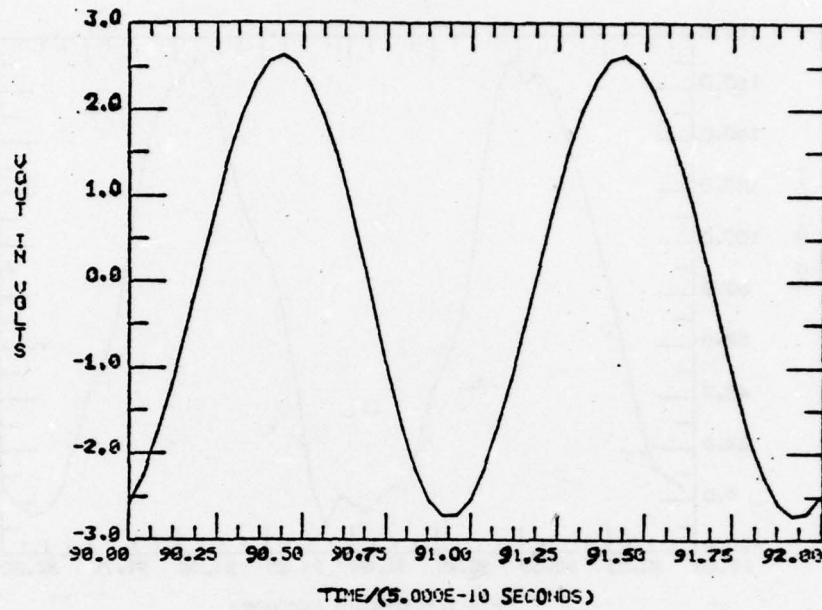
Figure 5.16 Drain to source voltage waveform

The above mentioned parasitic oscillations can be reduced by decreasing the value of L_1 . This causes the AC component of V_{DS} to decrease (the FET works into a low impedance load). It is also desirable to decrease the load resistance, R_L . This makes the structure more practical for high-frequency applications, in which 50Ω systems are utilized. Thus, the new design values chosen are (design number 2):

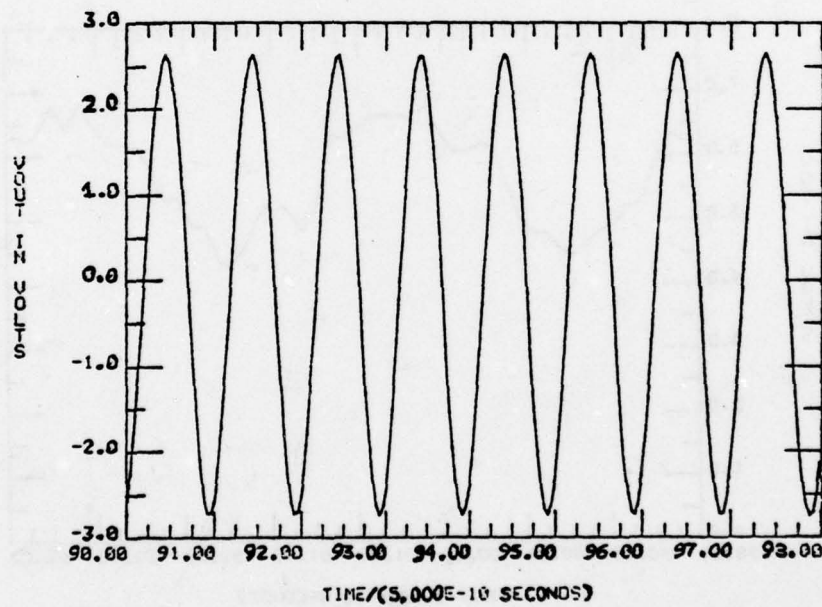
$$L_1 = 0.1\text{ nHy} , \quad R_L = 200\Omega$$

This design was checked by analyzing the network in the time domain, as described above. The steady-state waveforms are presented in Figure 5.17. From these Figures it is seen that the low frequency oscillation does not exist in the new design (Figure 5.17(b)). The high frequency oscillation still exists but it is greatly reduced compared to the previous design (compare Figure 5.15, 5.16 to 5.17(c), (d)). The output waveform distortion is very small. The Fourier analysis results are:

fundamental power	:	18.5 mW (12.7dbm)
second harmonic power	:	0.0033 mW (-24.8dbm)
third harmonic power	:	0.0024 mW (-26.2dbm)
total DC power dissipation:		428 mW



(a)



(b)

Figure 5.17 Oscillator waveforms (second design)
(a) output voltage (91st and 92nd cycles)
(b) output voltage (91st to 98th cycles)

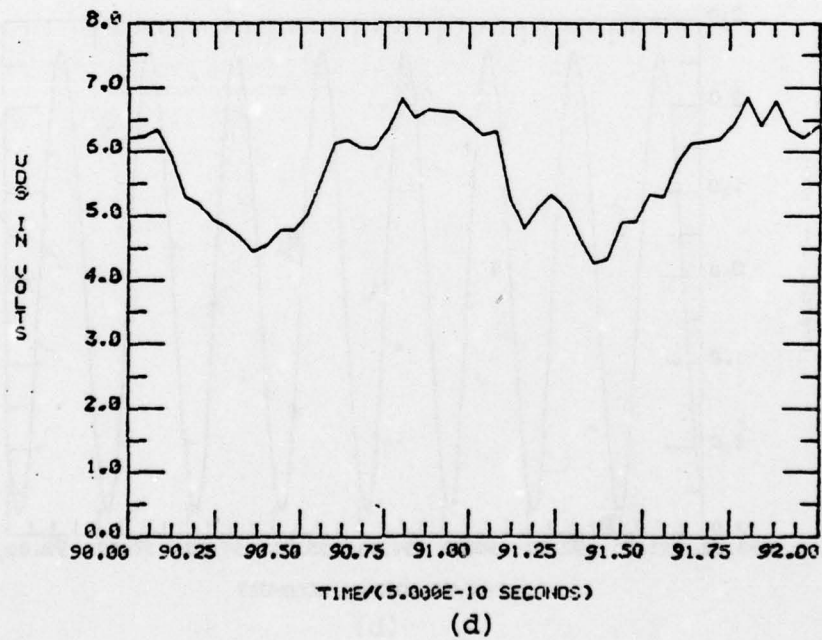
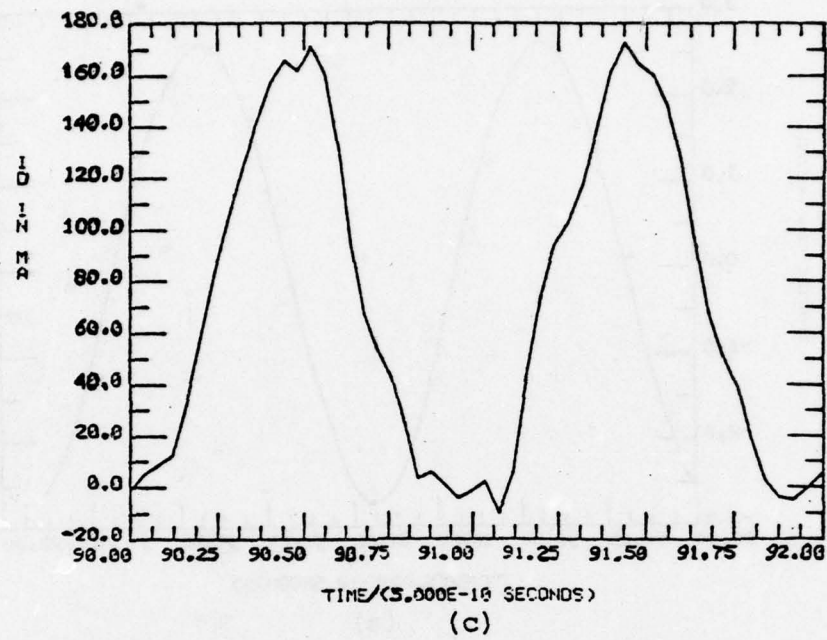


Figure 5.17 Oscillator waveforms (second design)
(c) drain current (d) drain to source voltage

Thus, less distortion was achieved with the new design. However, the output power for the new design is smaller, and the efficiency much worse (about 4.3%).

Several other designs were evaluated in an attempt to achieve better efficiency without low frequency oscillations. In addition to designs number 1 and 2, above, the following designs were analyzed:

design 3 - same as 2 except: $M=0.3\text{nHy}$, $R_L=500\Omega$

design 4 - same as 3 except: $V_{DD}=5\text{V}$

design 5 - same as 3 except: $V_{DD}=9\text{V}$

In Table 5.2 the performance of the various designs is summarized. It is seen that design number 4 has the best efficiency. Design number 3 has a slightly lower efficiency and slightly higher output power. All designs have good spectral purity. In the above simulations the average computation time per one cycle of the output voltage is about 2 minutes on the PDP-11/45. This corresponds to about 6 seconds on the IBM 360.

Table 5.2 Oscillator Performance

Design number	fundamental power mW (dbm)	second harmonic power mW (dbm)	third harmonic power mW (dbm)	DC power mW	efficiency %
1	24.3 (13.9)	0.035 (-14.6)	0.0069 (-21.6)	245	10
2	18.5 (12.7)	0.00329 (-24.8)	0.0024 (-26.2)	428	4.3
3	51 (17.1)	0.0242 (-16.2)	0.00728 (-21.4)	257	20
4	50.5 (17)	0.018 (-17.4)	0.00371 (-24.3)	228	22.1
5	49.8 (17)	0.00629 (-22)	0.00285 (-25.5)	394	12.6

6. SUMMARY AND CONCLUSIONS

In this report a new AC large signal model for the GaAs FET is presented. The model is based on basic principles, namely, electric field and charge transport in the device. The differential equations characterizing the device are formulated and their solution obtained. In contrast to previous simulations reported in the literature, the solution obtained here is analytic. This is achieved by introducing several approximations, the most important of which is assuming an analytical expression for the charge carrier concentration. The approximate analytic solution which results is quite close to the exact solution. However, to improve accuracy, corrective numerical iterations are employed as necessary.

The important effect of velocity saturation, which has a great impact on the device properties, is included in the model. Device operation is discussed and analyzed in terms of operational modes, which clarifies the physics of the device behavior. The model is "true" AC in the sense that the total terminal currents are computed as functions of the total terminal voltages and their time derivatives. The fact that the model is nearly analytic makes it very efficient and fast when implemented on a digital computer. Thus, the model is practical for the analysis and design of networks containing FETs.

The usefulness of the model is demonstrated in chapter 5, in which the computed FET performance is presented. The model is shown to be useful for small signal, DC and large signal analysis. The most important feature of the model is, of course, the large signal capability.

Summarized below are the main limitations of the new model, along with suggestions for future work, which may remove some of these limitations:

1) In the present form the model can be used for the doping level range: $5 \cdot 10^{15} \text{ cm}^{-3}$ to $2 \cdot 10^{17} \text{ cm}^{-3}$ (see appendix 8.3). This is not a basic limitation and depends on the approximation range in appendix 8.3. If necessary the range can be expanded by extending the above approximation. Similarly, the model uses the numerical values of the diffusion coefficients of GaAs. Thus it can be strictly used for GaAs only. However, the model can be easily modified for any material, by using the proper values for the diffusion coefficients.

2) The model can handle devices with uniform doping concentration only. This may be an important limitation in the future, since there is a present tendency to develop non-uniformly doped devices. (Investigators expect to improve the linearity and noise performance of the FET by the non uniform doping).

3) The model assumes an ideal substrate (namely, a perfect insulator). In practice, the substrate is not ideal, and there is some current conduction through it, resulting in power loss. Of course, the substrate loss can be handled as an external resistor, as done in Figure 4.1. A better representation of the substrate can be probably achieved, when the problem of non-uniform doping level is solved.

4) The model in its present form does not take into account the high field static Gunn domain present in the region between gate and drain as discussed in chapter 1. As shown in section 5.5 in the calculation of the small signal scattering parameters, the main effect of the static Gunn domain is to drop across it a large portion of the externally applied V_{DS} . Thus, the internal V_{DS} across the active gate region is generally small (the operating point near the knee). This decreases the gain (S_{21}) and the output impedance (S_{22}). To characterize the static domain, it is necessary to assume a domain shape and match the boundary conditions within the active gate region. As a first approximation it may be sufficient to introduce the voltage across the domain in the model. A better simulation of the domain could be achieved by considering also the domain impedance, which is generally a combination of resistance and capacitance in parallel.

The model presented in this report is a powerful tool for the analysis and design of components built with FETs. It allows, for the first time, the prediction of output power levels for large signal microwave components in practical circuits starting from a physical description of the FET device. Its use for analysis purposes is straightforward by following the instructions in chapter 4. The analysis results combined with an optimization program can be used to design networks with desired performance. Thus, the existence of this model should stimulate much network design research in the future.

7. ACKNOWLEDGMENTS

The authors wish to thank Mr. Harry Willing of the Naval Research Laboratory, Washington, D.C. for many helpful discussions, for making available to us his experimental results, and for his encouragement. Special thanks are due to Mr. Donald Green, Jr., of Washington University who aided in the interactive implementation of the FET model on the PDP 11/45 minicomputer, and who is proceeding to develop the program for efficient large-signal circuit simulation.

8. APPENDICES

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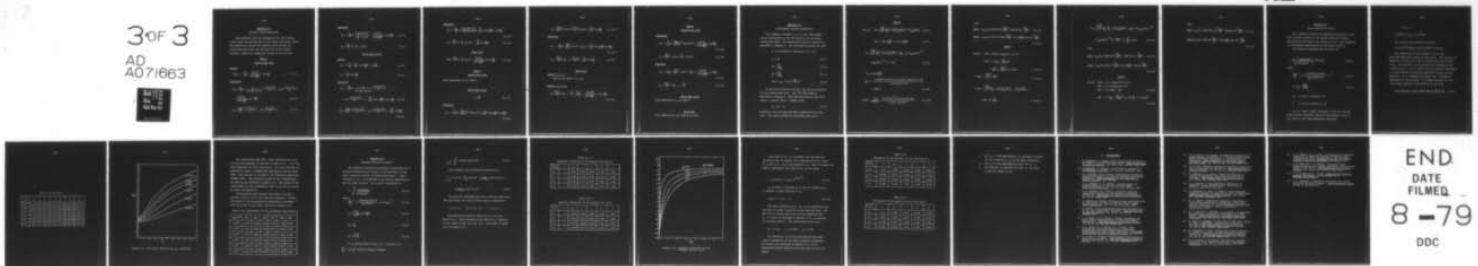
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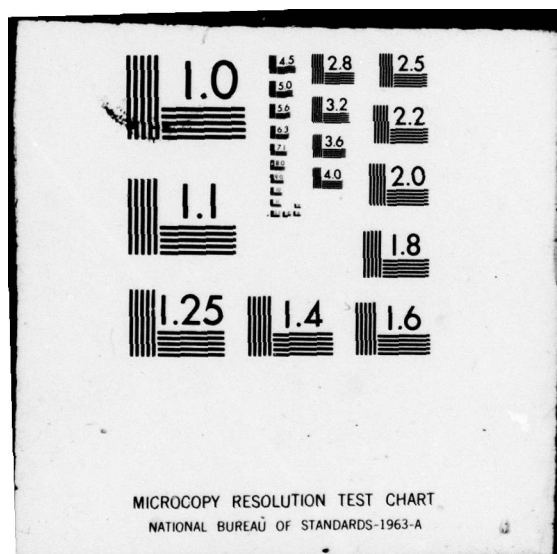
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Appendix 8.1

Electric Field Expressions

This appendix lists the expressions for the electric field inside the FET for each of the three operational modes. The expressions include the electric field on both the source and drain side, and for each one of the regions (channel, transition, depletion) as well as at the gate.

Mode A

source side (x=0)

channel

$$E=E_x = - \left[\frac{V_1}{l_g} + \frac{\pi V_o/2a}{\sinh(\frac{\pi l_g}{2a})} \cos \frac{\pi y}{2a} \right] \quad (8.1-1)$$

transition

$$E_x = - \left[\frac{V_1}{l_g} \left(1 - \frac{d}{2\pi(a - \frac{d}{2} - d_1(0))} \left\{ \frac{\pi(y-d_1(0))}{d} - \sin \frac{\pi(y-d_1(0))}{d} \right\} \right) + \frac{\pi V_o/2a}{\sinh(\frac{\pi l_g}{2a})} \cos \left(\frac{\pi y}{2a} \right) \right] \quad (8.1-2)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} \left[\frac{\pi(y-d_1(0))}{d} - \sin \frac{\pi(y-d_1(0))}{d} \right] \quad (8.1-3)$$

depletion

$$E_x = -\left[\frac{V_1}{lg}\left(1 - \frac{y-d/2-d_1(0)}{a-\frac{d}{2}-d_1(0)}\right) + \frac{\pi V_o/2a}{\sinh(\frac{\pi lg}{2a})} \cos\left(\frac{\pi y}{2a}\right)\right] \quad (8.1-4)$$

$$E_y = \frac{qN_D}{\epsilon} \left(y - \frac{d}{2} - d_1(0)\right) \quad (8.1-5)$$

drain side (x=lg)

channel

$$E_x = -\left[\frac{V_1}{lg} + \frac{\pi V_o}{2a} \coth\left(\frac{\pi lg}{2a}\right) \cos\left(\frac{\pi y}{2a}\right)\right] \quad (8.1-6)$$

$$E_y = \frac{\pi V_o}{2a} \sin\left(\frac{\pi y}{2a}\right) \quad (8.1-7)$$

transition

$$E_x = -\left[\frac{V_1}{lg}\left(1 - \frac{d}{2\pi(a-\frac{d}{2}-d_1(lg))} \left\{ \frac{\pi(y-d_1(lg))}{d} - \sin \frac{\pi(y-d_1(lg))}{d} \right\} + \frac{\pi V_o}{2a} \coth\left(\frac{\pi lg}{2a}\right) \cos\left(\frac{\pi y}{2a}\right)\right)\right] \quad (8.1-8)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} \left[\frac{\pi(y-d_1(lg))}{d} - \sin \frac{\pi(y-d_1(lg))}{d} \right] + \frac{\pi V_o}{2a} \sin\left(\frac{\pi y}{2a}\right) \quad (8.1-9)$$

depletion

$$E_x = -\left[\frac{V_1}{lg}\left(1 - \frac{y-d_1(lg)-d/2}{a-d_1(lg)-d/2}\right) + \frac{\pi V_o}{2a} \coth\left(\frac{\pi lg}{2a}\right) \cos\left(\frac{\pi y}{2a}\right)\right] \quad (8.1-10)$$

$$E_y = \frac{qN_D}{\epsilon} \left(y - \frac{d}{2} - d_1(lg)\right) + \frac{\pi V_o}{2a} \sin\left(\frac{\pi y}{2a}\right) \quad (8.1-11)$$

gate (y=a)

$$E=E_y = \frac{qN_D}{\epsilon} \left(a - \frac{d}{2} - d_1(x)\right) + \frac{\pi V_o/2a}{\sinh\left(\frac{\pi lg}{2a}\right)} \sinh\left(\frac{\pi x}{2a}\right) \quad (8.1-12)$$

Mode B

source side (x=0)

same expressions as for mode A.

drain side (x=lg)

$$\theta = \frac{\pi y}{d} \quad (8.1-13)$$

transition

$$E_x = -\left[\frac{V_1}{lg}\left(1 + \frac{qN_D}{4\epsilon\beta}\left(\frac{d}{\pi}\right)^2 \{2\cos\theta - \theta^2\}\right) + \left(\frac{\pi V_o}{2a}\right) \coth\left(\frac{\pi lg}{2a}\right) \cos\left(\frac{\pi y}{2a}\right)\right] \quad (8.1-14)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} [\theta - \sin\theta + \frac{V_1 - V_P}{\beta} (\theta + \sin\theta)] + \frac{\pi V_O}{2a} \sin(\frac{\pi y}{2a}) \quad (8.1-15)$$

depletion

$$E_x = -[\frac{V_1}{lg} (1 - \frac{qN_D d}{4\epsilon\beta} \{2y - d(1 - \frac{2}{\pi^2})\}) + \frac{\pi V_O}{2a} \coth(\frac{\pi lg}{2a}) \cos(\frac{\pi y}{2a})] \quad (8.1-16)$$

$$E_y = \frac{qN_D d}{2\epsilon} [2 \frac{y}{d} - 1 + \frac{V_1 - V_P}{\beta}] + \frac{\pi V_O}{2a} \sin(\frac{\pi y}{2a}) \quad (8.1-17)$$

gate (y=a)

region $0 < X < \gamma$

same as for mode A (8.1-12)

region $\gamma < X < lg$

$$E_y = \frac{qN_D d}{2\epsilon} [2 \frac{a}{d} - 1 - \frac{V_P}{\beta} + \frac{V_1 X}{\beta lg}] + \frac{(\pi V_O / 2a)}{\sinh(\frac{\pi lg}{2a})} \sinh(\frac{\pi X}{2a}) \quad (8.1-18)$$

Mode C

source side (x=0)

transition

$$E_x = -\left[\frac{V_1}{1g} \left(1 + \frac{qN_D d}{4\epsilon\beta} \left(\frac{d}{\pi} \right)^2 \{ 2\cos\theta - \theta^2 \} \right) + \frac{\pi V_O / 2a}{\sinh\left(\frac{\pi l g}{2a}\right)} \cos\left(\frac{\pi y}{2a}\right) \right] \quad (8.1-19)$$

$$E_y = \frac{qN_D d}{2\pi\epsilon} [\theta - \sin\theta - \frac{V_P}{\beta} (\theta + \sin\theta)] \quad (8.1-20)$$

depletion

$$E_x = -\left[\frac{V_1}{1g} \left(1 - \frac{qN_D d}{4\epsilon\beta} \left\{ 2y - d \left(1 - \frac{2}{\pi^2} \right) \right\} \right) + \frac{\pi V_O / 2a}{\sinh\left(\frac{\pi l g}{2a}\right)} \cos\left(\frac{\pi y}{2a}\right) \right] \quad (8.1-21)$$

$$E_y = \frac{qN_D d}{2\epsilon} \left[2 \frac{y}{d} - 1 - \frac{V_P}{\beta} \right] \quad (8.1-22)$$

drain side (x=lg)

same expressions as for mode B

gate (y=a)

same expression as for mode B (8.1-18)

Appendix 8.2

Displacement current expressions

This appendix includes a list of the displacement current expressions at the FET terminals in the three operational modes. The expressions have been derived as described in chapter 2. The following notations are used:

d, β as defined in Equations 2-13, 2-33

$$C_O \equiv \epsilon W \quad (8.2-1)$$

$$K1 \equiv \frac{\partial V_1}{\partial V_{SG}} \quad (8.2-2)$$

$$K2 \equiv \frac{\partial V_1}{\partial V_{DS}} \quad (8.2-3)$$

$$CD10 \equiv \phi_B - 0.0237 \frac{qN_D}{\epsilon} d^2 \quad (8.2-4)$$

$K1$ and $K2$ are functions of V_{SG} , V_{DS} and are different for each operational mode. They are calculated as described in chapter 3. The sign notations are gate and source - outward, drain - inward, thus:

$$I_S = I_D - I_G \quad (8.2-5)$$

Therefore, only the gate and drain expression are given here. The source current is calculated from 8.2-5.

Mode A

Define: $KGS = \sqrt{\frac{qN_D}{2\epsilon}} \frac{2lg}{V_1} (\sqrt{V_1 + V_{SG} + CD10} - \sqrt{V_{SG} + CD10}) \quad (8.2-6)$

$$KDS = [\cosh(\frac{\pi lg}{2a}) - 1] / \sinh(\frac{\pi lg}{2a}) \quad (8.2-7)$$

$$KG = \sqrt{\frac{qN_D}{2\epsilon}} \frac{2lg}{V_1} \{ \sqrt{V_1 + V_{SG} + CD10} - \frac{2}{3V_1} [(V_1 + V_{SG} + CD10)^{3/2} - (V_{SG} + CD10)^{3/2}] \} - KDS \quad (8.2-8)$$

$$KD = \coth(\frac{\pi lg}{2a}) - \frac{a}{lg} (1 - \frac{0.1487d^2 + 0.5a(a-d) - d_1(lg)[a - 0.5d_1(lg) - 0.5d]}{a(a - d_1(lg) - d/2)}) + CSG1A \quad (8.2-9)$$

$$CSG1A = \frac{\epsilon V_1}{2qN_D lg} \frac{[a - d_1(lg)]^2 + d(d_1(lg) - a + 0.2d)}{[a - \frac{d}{2} - d_1(lg)]^3} \quad (8.2-10)$$

then,

$$\text{gate: } I_{DIS} = C_O [(KGS + KG \cdot K1) \frac{dv_{SG}}{dt} + (KDS + KG \cdot K2) \frac{dv_{DS}}{dt}] \quad (8.2-11)$$

$$\text{drain: } I_{DIS} = C_O [- (KD \cdot K1 + CSG1A) \frac{dv_{SG}}{dt} + (\coth(\frac{\pi l g}{2a}) - KD \cdot K2) \frac{dv_{DS}}{dt}] \quad (8.2-12)$$

Mode B

Define: KDS = same as equation (8.2-7)

$$\begin{aligned} KDB = 1 - \frac{d}{lg} [1 - \frac{qN_D}{12\beta} d^2] - \\ - \frac{a-d}{lg} [1 - \frac{qN_D d}{4\epsilon\beta} (a + 0.2026d)] \end{aligned} \quad (8.2-13)$$

$$KGSC = \sqrt{\frac{qN_D}{\epsilon}} \frac{d \cdot lg}{\beta} \quad (8.2-14)$$

$$\begin{aligned} KGS = \sqrt{\frac{2qN_D}{\epsilon}} \frac{lg}{V_1} [\sqrt{V_P + V_{SG} + CD10} - \sqrt{V_{SG} + CD10}] + \\ + KGSC (1 - \frac{V_P}{V_1}) \end{aligned} \quad (8.2-15)$$

$$\begin{aligned}
 KG = & \sqrt{\frac{2qN_D}{\epsilon}} \frac{1g}{V_1} \left[\frac{V_P}{V_1} \sqrt{V_P + V_{SG} + CD10} - \frac{2}{3V_1} \{ (V_P + V_{SG} + CD10)^{3/2} \right. \\
 & \left. - (V_{SG} + CD10)^{3/2} \} \right] + \frac{KGSC}{2} \left(1 - \frac{V_P^2}{V_1^2} \right) - KDS \quad (8.2-16)
 \end{aligned}$$

then,

$$\text{gate: } I_{DIS} = C_O \left[(KGS + KG \cdot K1) \frac{dV_{SG}}{dt} + (KDS + KG \cdot K2) \frac{dV_{DS}}{dt} \right] \quad (8.2-17)$$

$$\begin{aligned}
 \text{drain: } I_{DIS} = & C_O \left[-KDB \cdot K1 \frac{dV_{SG}}{dt} + \left(\coth\left(\frac{\pi 1g}{2a}\right) - KDB \cdot K2 \right) \frac{dV_{DS}}{dt} \right] \\
 & (8.2-18)
 \end{aligned}$$

Mode C

Define: KGSC = as in Equation 8.2-14

KDS = as in Equation 8.2-7

$$KGC = 0.5 \cdot KGSC - KDS \quad (8.2-19)$$

$$\begin{aligned}
 KDC = & 1 - \frac{a}{1g} \left[1 - \frac{qN_D da}{4\epsilon\beta} \left(1 - 0.7974 \frac{d}{a} + 0.1307 \left(\frac{d}{a} \right)^2 \right) \right] \\
 & (8.2-20)
 \end{aligned}$$

then,

$$\text{gate: } I_{DIS} = C_O \left[(KGSC + KGC \cdot K1) \frac{dv_{SG}}{dt} + (KDS + KGC \cdot K2) \frac{dv_{DS}}{dt} \right] \quad (8.2-21)$$

$$\text{drain: } I_{DIS} = C_O \left[-KDC \cdot K1 \cdot \frac{dv_{SG}}{dt} + \left(\coth\left(\frac{\pi l g}{2a}\right) - KDC \cdot K2 \right) \frac{dv_{DS}}{dt} \right]$$

(8.2-22)

Appendix 8.3

Ratio Function For Mode C

This appendix contains the numerical calculation of the ratio function needed for the source conduction current approximation for mode C (see section 3.4.1). Also presented is a polynomial approximation to the above function.

The function considered here is given by:

$$R = \left[\int_0^{\pi} \frac{(1+\cos\theta)d\theta}{\sqrt{1+(E_y/E_x)^2}} \right] / [\tilde{\theta} + \sin\tilde{\theta}] \quad (8.3-1)$$

where,

$$\left(\frac{E_y}{E_x} \right)^2 = \left[A \frac{\theta - \sin\theta + K_c(\theta + \sin\theta)}{1 + K_{y1}(2\cos\theta - \theta^2)} \right]^2 \quad (8.3-2)$$

$$A = \frac{1}{S_1} = \frac{qN_D d}{2\pi\epsilon E_c} \quad (8.3-3)$$

K_{y1} is given in Equation 3-4

$\tilde{\theta}$ is given in Equation 3-46

K_{y1} is a small number (typically 0.02-0.03) and was found to have negligible effect on the function value in the range of the other parameters considered:

$$0 \leq K_C \leq 1$$

$$5 \cdot 10^{15} \text{ cm}^{-3} \leq N_D \leq 2 \cdot 10^{17} \text{ cm}^{-3}$$

The values of the constants used are:

$$q = 1.6 \cdot 10^{-19} \text{ coulomb}, E_C = 3.2 \cdot 10^5 \text{ V/m}, \epsilon = 12.5 \epsilon_0.$$

The computation of the integral in 8.3-1 was performed numerically using 100 partitions. The results are presented in Table 8.3-1 for 11 values of K_C and 6 values of N_D . The same data is also presented in graphical form in Figure 8.3-1. It is evident that the function considered is a monotonically increasing function of both K_C and N_D . Therefore, it is reasonable to assume that a polynomial approximation can be found. An attempt was made to find a fifth order polynomial approximation of the form:

$$R(K_C) = RRO + RR1 \cdot K_C + RR2 \cdot K_C^2 + RR3 \cdot K_C^3 + RR4 \cdot K_C^4 + RR5 \cdot K_C^5 \quad (8.3-4)$$

Table 8.3-1 The ratio function

K_c $N_D (\text{cm}^{-3})$	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
$5 \cdot 10^{15}$	1.095	1.132	1.207	1.325	1.473	1.632	1.790	1.941	2.081	2.212	2.333
$1 \cdot 10^{16}$	1.129	1.210	1.356	1.572	1.814	2.063	2.292	2.508	2.700	2.890	3.054
$3 \cdot 10^{16}$	1.170	1.325	1.617	1.954	2.279	2.571	2.830	3.044	3.262	3.443	3.606
$6 \cdot 10^{16}$	1.219	1.459	1.883	2.308	2.672	2.986	3.230	3.468	3.663	3.839	4.000
$1 \cdot 10^{17}$	1.230	1.559	2.065	2.525	2.909	3.222	3.472	3.693	3.906	4.075	4.238
$2 \cdot 10^{17}$	1.263	1.731	2.378	2.895	3.295	3.616	3.884	4.115	4.318	4.500	4.664

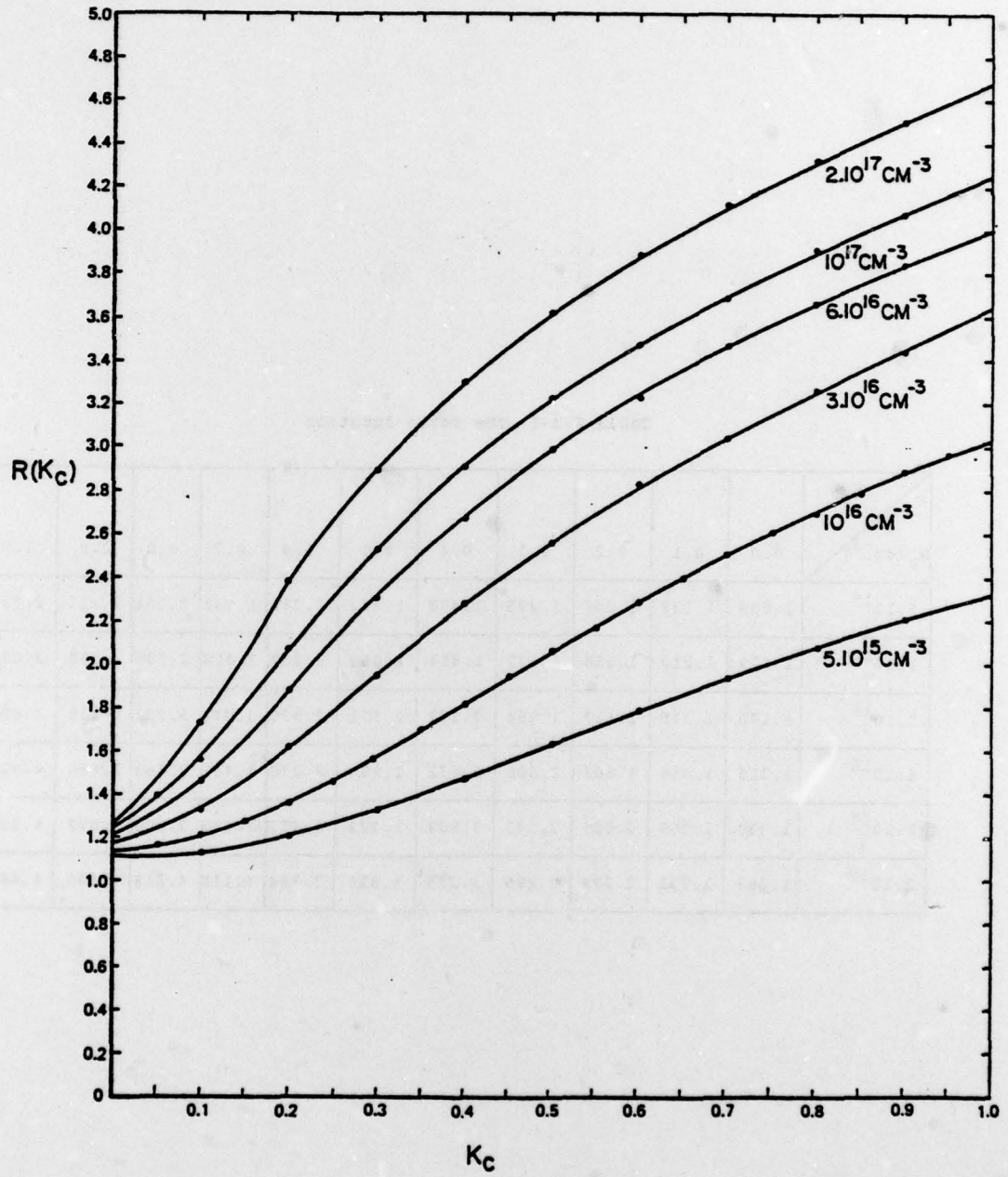


Figure 8.3-1 The ratio function (N_D as a parameter)

The coefficients $RR0, RR1, \dots$ were determined by curve fitting the polynomial to the data in Table 8.3-1. This was done separately for each value of N_D . The curve fitting was achieved by using a standard IBM optimization routine named FMCG. This routine is included in the Scientific Subroutine Package (SSP). The resulting values of the 6 coefficients for each N_D are presented in Table 8.3-2. The values of the coefficients for any intermediate value of N_D are calculated by linear interpolation.

The polynomial approximation was found to be very accurate (within 2-3% of the numerical solution). In fact, the graphs of the polynomials are practically coincident with the graphs of the actual function in Figure 8.3-1.

Table 8.3-2 Coefficients for the polynomial approximation

$N_D (\text{cm}^{-3})$	RR0	RR1	RR2	RR3	RR4	RR5
5.10^{15}	1.095	0.066	2.824	-1.123	-1.510	0.982
1.10^{16}	1.129	0.364	4.621	-2.457	-2.665	2.065
3.10^{16}	1.170	1.464	4.992	-3.833	-3.162	2.982
6.10^{16}	1.219	2.652	4.481	-4.894	-2.806	3.362
1.10^{17}	1.230	3.740	3.138	-5.429	-0.957	2.531
2.10^{17}	1.263	5.702	-0.443	-3.179	-0.559	1.895

Appendix 8.4

Integral Function For Mode C

This appendix contains the numerical calculation of an integral function which is part of the expression of the drain conduction current for operational mode C - case 2 (section 3.4.2). Also derived is an analytic approximation for the above function. The function considered is

$$I = \int_0^{\pi} \frac{(1+\cos\theta)d\theta}{\sqrt{1+(E_y/E_x)^2}} \quad (8.4-1)$$

where:

$$\left(\frac{E_y}{E_x}\right)^2 = \left[\frac{\theta - \sin\theta + l_3(\theta + \sin\theta)}{l_1 \cos(l_2\theta)} + \tan(l_2\theta) \right]^2 \quad (8.4-2)$$

$$l_1 = \frac{\pi^2 \epsilon V_0}{q N_D d a} \coth\left(\frac{\pi l g}{2a}\right) \quad (8.4-3)$$

$$l_2 = \frac{d}{2a} \quad (8.4-5)$$

$$l_3 = \frac{V_1 - V_P}{\beta} \quad (8.4-6)$$

It is obvious that $I \rightarrow 0$ for $l_1 \rightarrow 0$. Also for $l_1 \rightarrow \infty$

$\frac{E_y}{E_x} \rightarrow \tan(l_2\theta)$ and the integral becomes:

$$I = \int_0^{\pi} (1 + \cos \theta) \cos(\ell_2 \theta) d\theta \quad (8.4-7)$$

This integral can be evaluated analytically:

$$I = \mu_1(\ell_2) = \frac{1}{\ell_2} \sin(\ell_2 \pi) + \frac{1}{2(1+\ell_2)} \sin[(1+\ell_2)\pi] + \frac{1}{2(1-\ell_2)} \sin[(1-\ell_2)\pi] \quad (8.4-8)$$

The function considered here was evaluated numerically (100 partitions) for the following range of parameters:

$$0 \leq \ell_1 \leq 5, \quad \ell_2 = 0.15, 0.4, \quad 0 \leq \ell_3 \leq 1$$

The results are given in Table 8.4-1, 8.4-2 and Figure 8.4-1. Also included is the value of μ_1 (Equation 8.4-8), which is the limit for $\ell_1 \rightarrow \infty$. This limit is shown also in Figure 8.4-1.

Table 8.4 -1

Numerical evaluation of the integral for $\ell_2=0.15$

$\ell_3 \backslash \ell_1$	0	0.1	1	2	5	∞
0.0	0	1.955	2.819	2.956	3.047	3.096
0.3	0	0.936	2.421	2.744	2.971	3.096
0.6	0	0.651	2.077	2.522	2.882	3.096
1.0	0	0.494	1.743	2.256	2.755	3.096

Table 8.4-2

Numerical evaluation of the integral for $\ell_2=0.4$

$\ell_3 \backslash \ell_1$	0	0.1	1	2	5	∞
0.0	0	1.828	2.543	2.665	2.758	2.831
0.3	0	0.892	2.163	2.438	2.656	2.831
0.6	0	0.627	1.869	2.236	2.557	2.831
1.0	0	0.479	1.587	2.010	2.432	2.831

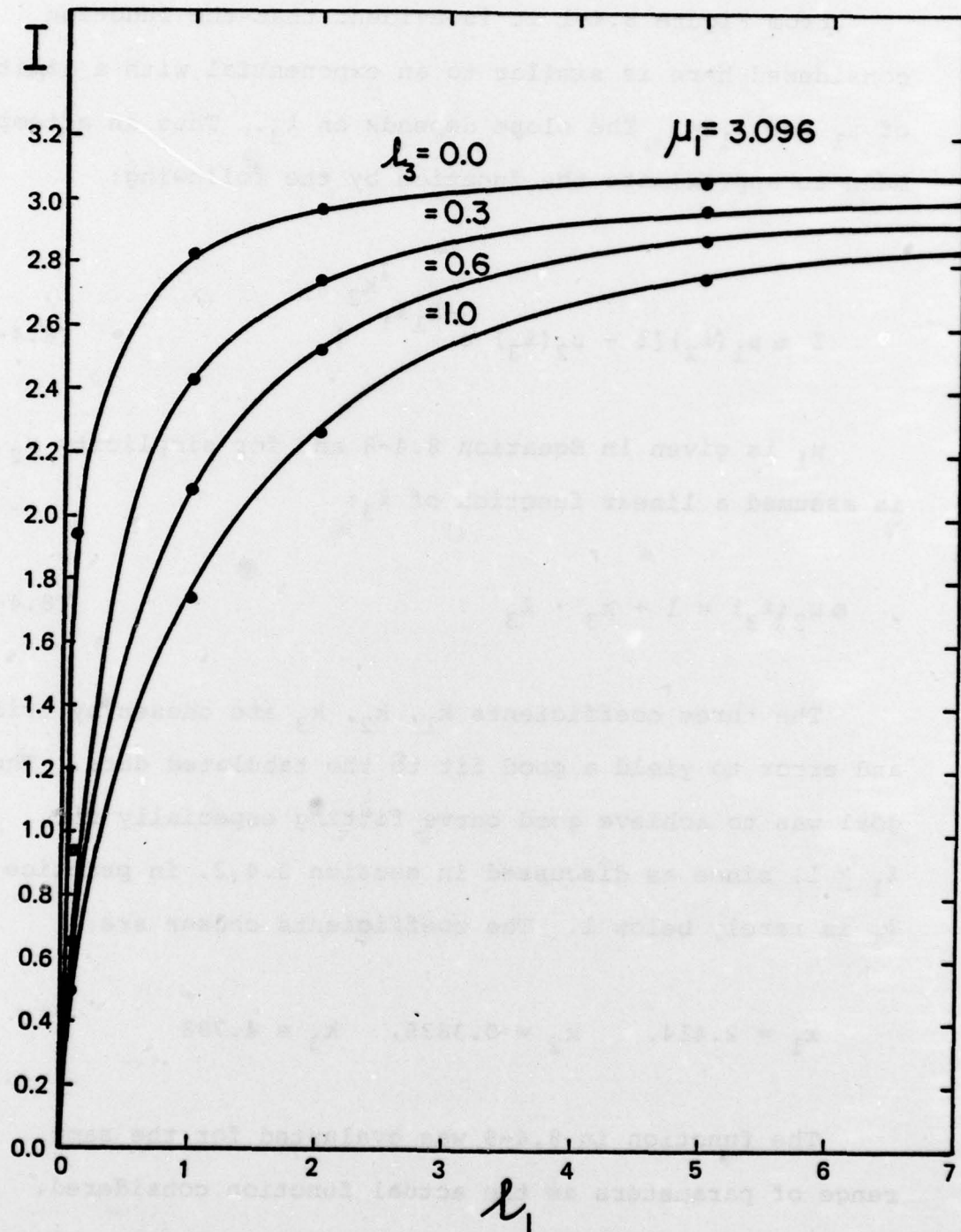


Figure 8.4-1 Numerical evaluation of the integral for $l_2 = 0.15$

From Figure 8.4-1 it is evident that the function considered here is similar to an exponential with a limit of μ_1 for $\ell_1 \rightarrow \infty$. The slope depends on ℓ_3 . Thus an attempt was made to approximate the function by the following:

$$I \approx \mu_1(\ell_2) [1 - \mu_2(\ell_3) e^{-k_1 \ell_1^{k_2}}] \quad (8.4-9)$$

μ_1 is given in Equation 8.4-8 and for simplicity μ_2 is assumed a linear function of ℓ_3 :

$$\mu_2(\ell_3) = 1 + k_3 \cdot \ell_3 \quad (8.4-10)$$

The three coefficients k_1 , k_2 , k_3 are chosen by trial and error to yield a good fit to the tabulated data. The goal was to achieve good curve fitting especially for $\ell_1 \geq 1$, since as discussed in section 3.4.2, in practice ℓ_1 is rarely below 1. The coefficients chosen are:

$$k_1 = 2.414, \quad k_2 = 0.3835, \quad k_3 = 4.798$$

The function in 8.4-9 was evaluated for the same range of parameters as the actual function considered. The results are tabulated in Tables 8.4-3, 8.4-4. Comparison between Tables 8.4-1, 8.4-3 and 8.4-2, 8.4-4 shows:

Table 8.4-3

Evaluation of the function in 8.4-9 for $l_2=0.15$

$l_3 \backslash l_1$	0	0.1	1	2	5
0.0	0.0	1.955	2.819	2.964	3.061
0.3	-4.456	0.313	2.421	2.772	3.010
0.6	-8.913	-1.330	2.022	2.581	2.960
1.0	-14.855	-3.520	1.490	2.326	2.892

Table 8.4-4

Evaluation of the function in 8.4-9 for $l_2=0.4$

$l_3 \backslash l_1$	0	0.1	1	2	5
0.0	0.0	1.787	2.577	2.709	2.798
0.3	-4.075	0.286	2.213	2.534	2.750
0.6	-8.150	-1.215	1.848	2.360	2.705
1.0	-13.583	-3.217	1.362	2.127	2.644

1. For $l_3 = 0$ the approximation is reasonably accurate for all values of l_1, l_2 in the range considered.
2. For $l_3 \neq 0$ the approximation fails for $l_1 < 1$.
3. The accuracy is improved the lower l_3 , the lower l_2 and the higher l_1 are.

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